500MHz-2GHz BROADBAND POWER AMPLIFIER DESIGN BY NON-LINEAR MODELING METHODS

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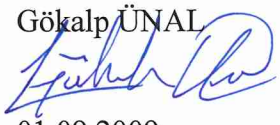
Signature	:	
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ABSTRACT

500MHz-2GHz BROADBAND POWER AMPLIFIER DESIGN BY NON-LINEAR MODELING METHODS

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This thesis presents the design methods of 500MHz-2GHz broadband RF power amplifier. First of all, RF power transistor technologies are searched and the most suitable one is chosen according to its operation of frequency band, maximum output power, efficiency and cost features. The amplifier is designed as it has two stages, and in both stages LDMOS transistor technology is used as RF power transistors. Large signal models for the LDMOS devices are used in simulation, and according to the measurement results, the circuitry in simulation is tried to model at nonlinear conditions. A broadband RF-Choke structure with a new technique is developed to obtain high DC isolation and low RF loss over the desired bandwidth. Input and output matching networks and shunt feedback topology are introduced to fulfill the bandwidth requirements. Typical values of 20dB power gain, 37dBm output power, have been achieved at the most part of the frequency band of 500MHz-2GHz.

Keywords: RF, power amplifier, RF-Choke, transistor technologies, non-linear modeling

ÖZ

DOĞRUSAL OLMAYAN MODELLEME YÖNTEMİYLE 500MHz-2GHz GENİŞ BANTLI GÜÇ YÜKSELTEÇ TASARIMI

ÜNAL, Gökalp
Yüksek Lisans, Elektronik ve Haberleşme Mühendisliği Anabilim Dalı
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Bu tez 500MHz-2GHz geniş bantlı RF güç yükseltecin tasarım yöntemlerini göstermektedir. İlk olarak, RF güç transistör teknolojileri araştırıldı ve içlerinden çalışma bandına, en yüksek çıkış gücüne, verimliliğine ve fiyatına göre en uygun olanı seçildi. Güç yükselteç iki aşama olacak şekilde tasarlandı ve bu iki aşamada da RF güç transistörü olarak LDMOS teknolojisi kullanıldı. Benzetimde LDMOS elemanları için yüksek sinyal modelleri kullanıldı ve ölçüm sonuçlarına göre benzetimdeki devre doğrusal olmayan durumda modellenmeye çalışıldı. İstenen bantta yüksek doğru akım yalıtımı ve düşük RF kaybı elde edebilmek için yeni bir teknik ile geniş bantlı RF yüksek frekans söndürme bobini yapısı geliştirildi. Bütün banttaki gereksinimleri sağlamak için giriş ve çıkış uyumlama devreleri ve paralel geri besleme yapısı kullanıldı. 500MHz-2GHz bandının büyük bir kısmında, tipik değerler olarak 20dB güç kazancı ve 37dBm çıkış gücü elde edildi.

Anahtar Kelimeler: RF, güç yükselteç, RF yüksek frekans söndürme bobini, transistör teknolojileri, doğrusal olmayan modelleme

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CHAPTER I

INTRODUCTION

This thesis presents design methods of two stage 5W broadband amplifier covering the frequency range from 500MHz to 2GHz. Power amplifier design is explained theoretically in next chapter. In third chapter, brief information of transistor technologies is given and comparable tables and charts are showed.

The design features are tried to obtain in two stage power amplifier configuration. In chapter four, single stage design process is explained. Si LDMOS is used in driver and also in last stage. Large signal models are used for the LDMOS devices. PCB materials are searched and the most suitable one (Rogers RO4003C) is selected. A broadband choke structure is developed to obtain high dc isolation and low RF loss over the full bandwidth. In chapter five, multi stage (complete system) design process is explained. Broadband input and output matching networks and shunt feedback topology are introduced to fulfill the bandwidth requirements.

Typical values of 20dB power gain, 37dBm output power, have been achieved in most part of the frequency band of 500MHz-2GHz. All power and linearity results are obtained at the whole frequency band. The design procedure is given in detail and the measurement results are discussed and also compared with simulations.

CHAPTER II

HIGH POWER RF TRANSISTOR AMPLIFIER DESIGN

It is quite common for new designers to design amplifier with “large signal” analysis. The distinction is quite important because prior to 1985, large-signal analysis was rarely applied to circuits because of its difficulty and the lack of simulation tools. The wealth of analysis centers around S-parameter analysis and equivalent linear characterization of devices, is so tractable and amenable to application that even today we attempt to apply this body of knowledge to components that are clearly large signal in their operation. S-parameters are based upon matrix algebra and the linear addition of incident and reflected voltages. By definition, therefore, they are a linear technique for describing the device. The device being described is assumed invariant to the magnitude (or phase) of the incident and reflected voltages. The attempt to apply them to a device that clearly does not fall into this category is known as quasi-linear analysis. It is needed to be clear about what does it mean by a nonlinear circuit and its impact on component operation [1].

2.1. LOAD LINE ANALYSIS

A load line is a technique for finding the optimum impedance to present to the output stage of the power amplifier. If we look at the $I-V$ curves for a FET, we see that there is a useable region for both drain current and drain-to-source voltage.

To keep the output voltage within the linear region of the FET, we avoid the steep-sloped areas of the $I-V$ curves [2].

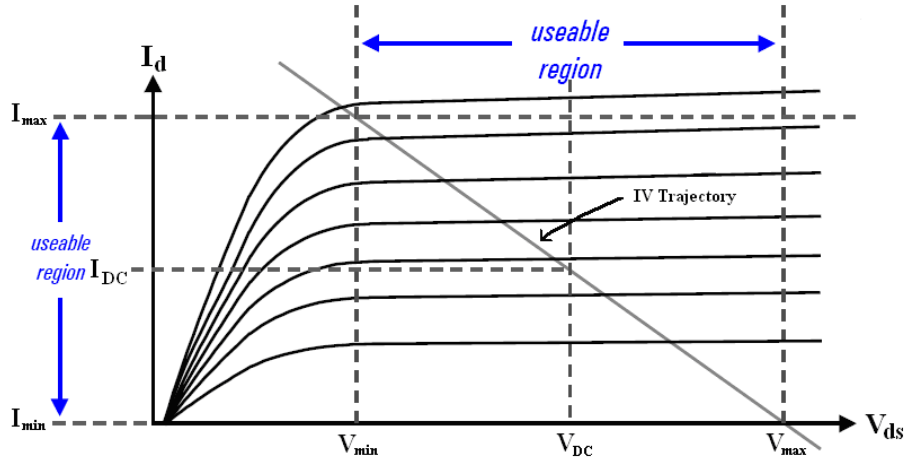

Figure 2.1: A simple load line for class-A application

As seen from the above figure, useable regions for V_{ds} and I_d are needed to be used for linear operation. It is important to put a transistor's load line in these regions, because of reducing non-linear effects. Following formulas show what output impedance should be to obtain optimum load line swing for class-A application.

$$V_{RMS} = \frac{V_{\max} - V_{\min}}{2\sqrt{2}} \tag{2.1}$$

$$I_{RMS} = \frac{I_{\max} - I_{\min}}{2\sqrt{2}} \tag{2.2}$$

then,

$$P_{LOAD} = V_{RMS} I_{RMS} \tag{2.3}$$

so,

$$P_{LOAD} = \frac{(V_{\max} - V_{\min})(I_{\max} - I_{\min})}{8} \tag{2.4}$$

where P_{LOAD} is known according to the specification of design. $V_{\max}$ and $V_{\min}$ can be found from DC analysis of a transistor. $I_{\min}$ is approximately 0 for RF power transistors. So, R_L can be found

$$R_L = \frac{(V_{\max} - V_{\min})}{(I_{\max} - I_{\min})} \tag{2.5}$$

from the above formula [3].

According to the figure these relations can be said.

- Slope of a load line is related with the value of R_L,
- position of a load line in y-axis is related with V_{GS} (biasing point),
- length of a load line is related with P_{in} (input power).

So, load line of a transistor is adjusted according to the above relations.

2.2. STABILITY CONSIDERATIONS

The stability of an amplifier, or its resistance to oscillate, is a very important consideration in a design and can be determined from the S parameters, the matching networks, and the terminations. In a two-port network, oscillations are possible when either the input or output port presents a negative resistance. This occurs when $|\Gamma_{IN}| > 1$ or $|\Gamma_{OUT}| > 1$, which for a unilateral device occurs when $|S_{11}| > 1$ or $|S_{22}| > 1$.

The two-port network shown in Figure 2.2 is said to be unconditionally stable at a given frequency if the real parts of Z_{IN} and Z_{OUT} are greater than zero for all passive load and source impedances. If the two-port is not unconditionally stable, it

is potentially unstable. That is, some passive load and source terminations can produce input and output impedances having a negative real part.

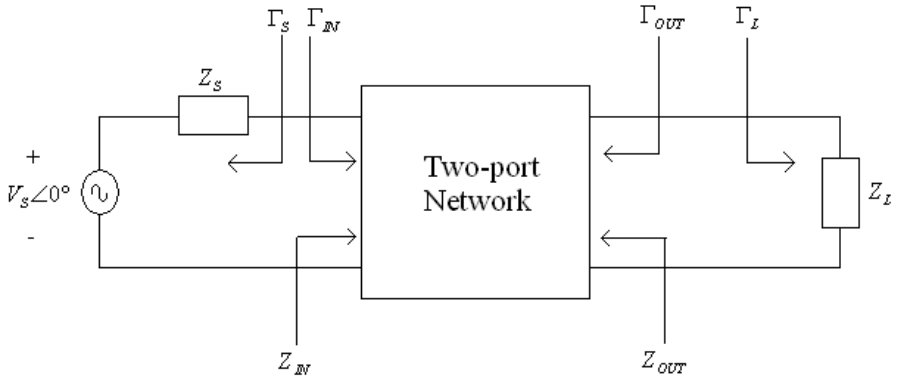

Figure 2.2: Stability of two port network

In terms of reflection coefficients, the conditions for unconditional stability at a given frequency are

$$\left|\Gamma_S\right| < 1 \tag{2.6}$$

$$\left|\Gamma_L\right| < 1 \tag{2.7}$$

$$\left|\Gamma_{IN}\right| = \left|S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L}\right| < 1 \tag{2.8}$$

and

$$\left|\Gamma_{OUT}\right| = \left|S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S}\right| < 1 \tag{2.9}$$

where, of course, all coefficients are normalized to the same characteristic impedance Z_0.

The solutions of (2.6) to (2.7) give the required conditions for the two-port network to be unconditionally stable [4].

Condition (2.8) can be rearranged as follows:

$$\left| S_{11} + \frac{S_{22}S_{12}S_{21}\Gamma_L + \left(S_{12}S_{21} - S_{12}S_{21}\right)}{S_{22}\left(1 - S_{22}\Gamma_L\right)} \right| < 1 \tag{2.10}$$

or,

$$\left| \frac{1}{S_{22}} \left(\Delta + \frac{S_{12}S_{21}}{1 - S_{22}\Gamma_L} \right) \right| < 1 \tag{2.11}$$

where,

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{2.12}$$

after some manipulations,

$$1 - \left|S_{22}\right|^2 - \left|S_{12}S_{21}\right| > 0 \tag{2.13}$$

similarly, stability condition (2.9) will be satisfied if

$$1 - \left|S_{11}\right|^2 - \left|S_{12}S_{21}\right| > 0 \tag{2.14}$$

adding (2.13) and (2.14), we get

$$2 - \left|S_{11}\right|^2 - \left|S_{22}\right|^2 - 2\left|S_{12}S_{21}\right| > 0 \tag{2.15}$$

or,

$$1 - \frac{1}{2}\left(\left|S_{11}\right|^2 - \left|S_{22}\right|^2\right) > 2\left|S_{12}S_{21}\right| \tag{2.16}$$

from (2.12) and (2.16), we have

$$\left|\Delta\right| < \left|S_{11}S_{22}\right| + \left|S_{12}S_{21}\right| < \left|S_{11}S_{22}\right| + 1 - \frac{1}{2}\left(\left|S_{11}\right|^2 - \left|S_{22}\right|^2\right) \tag{2.17}$$

or,

$$\left|\Delta\right| < 1 - \frac{1}{2}\left(\left|S_{11}\right| - \left|S_{22}\right|\right)^2 \Rightarrow \left|\Delta\right| < 1 \tag{2.18}$$

on the other hand,

$$1-|S_{11}|^2-|S_{22}|^2-2|S_{12}S_{21}|+|\Delta|^2>0 \tag{2.19}$$

or,

$$1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2>2|S_{12}S_{21}| \tag{2.20}$$

or,

$$\frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{12}S_{21}|}>1 \tag{2.21}$$

therefore,

$$k=\frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{12}S_{21}|}>1 \tag{2.22}$$

If S-parameters of a transistor satisfy conditions (2.18) and (2.22) then it is stable for any passive load and generator impedance. In other words, this transistor is *unconditionally stable*. On the other hand, it may be conditionally stable (stable for limited values of load or source impedance) if one or both of these conditions are violated. It means that the transistor can provide stable operation for a restricted range of Γ_S and Γ_L.

2.3. IMPEDANCE MATCHING NETWORKS

One of the most critical requirements in the design of high-frequency electronic circuits is that the maximum possible signal energy is transferred at each point. In other words, the signal should propagate in a forward direction with a negligible echo (ideally, zero). Echo signal not only reduces the power available but also deteriorates the signal quality due to the presence of multiple reflections. Impedance can be transformed to a new value by adjusting the turn ratio of a transformer that couples it with the circuit. However, it has several limitations. In

this section a few techniques to design other impedance transforming networks are presented. These circuits include transmission line stubs, and resistive and reactive networks. Further, the techniques introduced are needed in active circuit design at RF and microwave frequencies.

As shown in Figure 2.3, impedance matching networks are employed at the input and the output of an amplifier circuit. These networks may also be needed to perform some other tasks, such as filtering the signal and blocking or passing the dc bias voltages. This section begins with impedance matching techniques that use a single reactive element or stub connected in series or in shunt. Theoretical principles

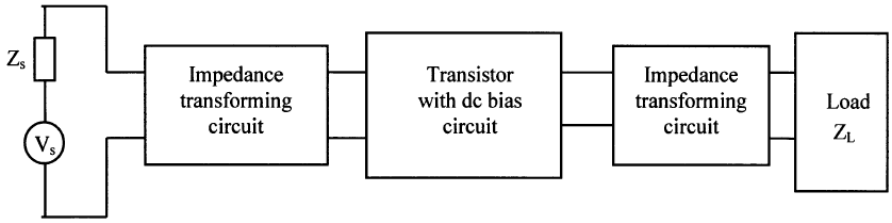

Figure 2.3: Block diagram of an amplifier circuit

behind the technique are explained.

Single Reactive Element or Stub Matching

When a lossless transmission line is terminated by an impedance Z_L, the magnitude of the reflection coefficient (and hence, the VSWR) on it remains constant but its phase angle can be anywhere between $+180°$ and $-180°$. As one moves away from the load, impedance (or the admittance) value changes. This movement is clockwise on the VSWR circle. The real part of the normalized impedance (or the normalized admittance) becomes unity at certain points on the line. Addition of a single reactive element or a transmission line stub at this point can eliminate the

echo signal and reduce the VSWR to unity beyond this point. A finite-length transmission line with its other end open or short circuit is called the stub and behaves like a reactive element.

In this section, the procedure for determining the location on a lossless feeding line is discussed where a stub or a reactive element can be connected to eliminate the echo signal. Two different possibilities, a series or a shunt element, are considered.

A Shunt Stub or Reactive Element

Consider a lossless transmission line of characteristic impedance Z_0 that is terminated by a load admittance Y_L, as shown in Figure 2.4. Corresponding normalized input admittance at a point d_s away from the load can be found from as follows:

$$\overline{Y}_{in} = \frac{\overline{Y}_L + j\tan(\beta d_s)}{1 + j\overline{Y}_L \tan(\beta d_s)} \tag{2.23}$$

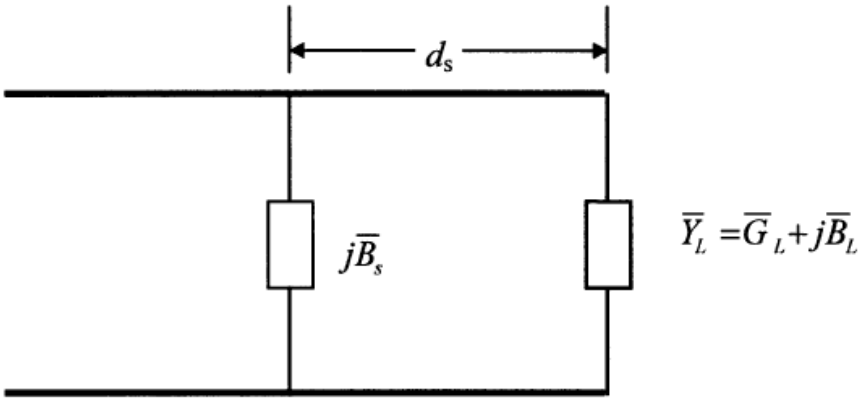

Figure 2.4: Transmission line with a shunt matching element

In order to obtain a matched condition at d_s, the real part of the input admittance must be equal to the characteristic admittance of the line; i.e., the real part of (2.23)

must be unity. This requirement is used to determine d_s. The parallel susceptance B_s is then connected at d_s to cancel out the imaginary part of Y_{in}. Hence,

$$ds = \frac{1}{\beta}\tan^{-1}\left(\frac{\overline{B}_L \pm \sqrt{\overline{B}_L{}^2 - A\left(1-\overline{G}_L\right)}}{A}\right) \tag{2.24}$$

where $A = \overline{G}_L\left(\overline{G}_L - 1\right) + B_L{}^2$.

The imaginary part of the normalized input admittance at d_s is found as follows.

$$\overline{B}_{in} = \frac{\left\{\overline{B}_L + \tan\left(\beta d_s\right)\right\}\times\left\{1 - \overline{B}_L\tan\left(\beta d_s\right)\right\} - \overline{G}_L{}^2\tan\left(\beta d_s\right)}{\left\{\overline{G}_L\tan\left(\beta d_s\right)\right\}^2 + \left\{1 - \overline{B}_L\tan\left(\beta d_s\right)\right\}^2} \tag{2.25}$$

The other requirement to obtain a matched condition is

$$\overline{B}_s = -\overline{B}_{in} \tag{2.26}$$

Hence, shunt inductor is needed at d_s if the input admittance is found capacitive (i.e., $\overline{B}_{in}$ is positive). On the other hand, it will require a capacitor if Y_{in} is inductive at d_s. A lossless transmission line section can be used in place of this inductor or capacitor. Length of this transmission line section is determined according to the susceptance needed by (2.26) and the termination (i.e., an open circuit or a short circuit) at its other end. This transmission line section is called a *stub*. If ℓ_s is the stub length that has a short circuit at its other end, then

$$\ell_s = \frac{1}{\beta}\cot^{-1}(-\overline{B}_s) = \frac{1}{\beta}\cot^{-1}(-\overline{B}_{in}) \tag{2.27}$$

On the other hand, if there is an open circuit at the other end of the stub, then

$$\ell_s = \frac{1}{\beta}\tan^{-1}(\overline{B}_s) = \frac{1}{\beta}\tan^{-1}(-\overline{B}_{in}) \tag{2.28}$$

A Series Stub or Reactive Element

If a reactive element (or a stub) needs to be connected in series as shown in Figure 2.5, the design procedure can be developed as follows. The normalized input impedance at d_s is

$$\overline{Z}_{in} = \frac{\overline{Z}_L + j\tan(\beta d_s)}{1 + j\overline{Z}_L \tan(\beta d_s)} \tag{2.29}$$

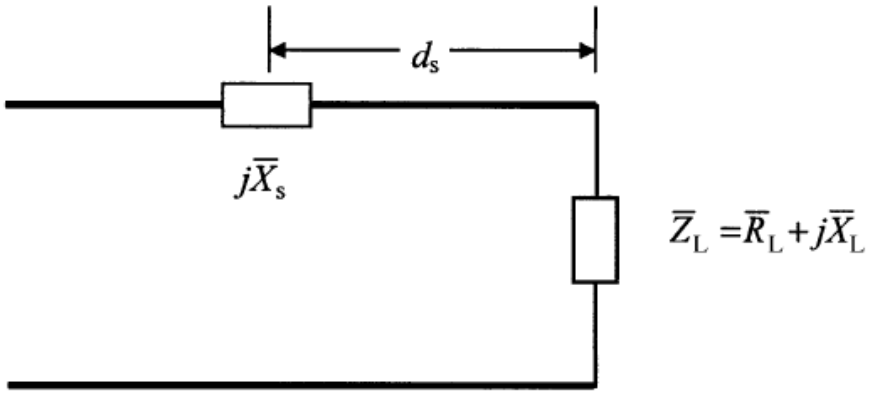

Figure 2.5: Transmission line with a matching element connected in series

In order to obtain a matched condition at d_s, the real part of the input impedance must be equal to the characteristic impedance of the line; i.e., the real part of (2.29) must be unity. This condition is used to determine d_s. A reactance X_s is then connected in series at d_s to cancel out the imaginary part of Z_{in}. Hence,

$$d_s = \frac{1}{\beta}\tan^{-1}\left(\frac{\overline{X}_L \pm \sqrt{\overline{X}_L{}^2 - A_z\left(1-\overline{R}_L\right)}}{A_z}\right) \tag{2.30}$$

where $A_z = \overline{R}_L\left(\overline{R}_L - 1\right) + \overline{X}_L{}^2$.

The imaginary part of the normalized input impedance at d_s is found as follows.

$$\overline{X}_{in} = \frac{\left\{\overline{X}_L + \tan\left(\beta d_s\right)\right\}\times\left\{1 - \overline{X}_L\tan\left(\beta d_s\right)\right\} - \overline{R}_L{}^2\tan\left(\beta d_s\right)}{\left\{\overline{R}_L\tan\left(\beta d_s\right)\right\}^2 + \left\{1 - \overline{X}_L\tan\left(\beta d_s\right)\right\}^2} \tag{2.31}$$

In order to obtain a matched condition at d_s, the reactive part X_{in} must be eliminated by adding an element of opposite nature. Hence,

$$\overline{X}_s = -\overline{X}_{in} \tag{2.32}$$

Therefore, a capacitor will be needed in series if the input impedance is inductive. It will require an inductor if input reactance is capacitive. A transmission line stub can be used instead of an inductor or a capacitor. Length of this stub with an open circuit at its other end can be determined as follows.

$$\ell_s = \frac{1}{\beta}\cot(-\overline{X}_s) = \frac{1}{\beta}\cot(-\overline{X}_{in}) \tag{2.33}$$

However, if the stub has a short circuit at its other end, its length will be a quarter-wavelength shorter (or longer, if the resulting number becomes negative) than this value. It can be found as

$$\ell_s = \frac{1}{\beta}\tan(\overline{X}_s) = \frac{1}{\beta}\tan(-\overline{X}_{in}) \tag{2.34}$$

Note that the location d_s and the stub length ℓ_s are periodic in nature in both cases. It means that the matching conditions will also be satisfied at points one-half wavelength apart. However, the shortest possible values of d_s and ℓ_s are preferred because those provide the matched condition over a broader frequency band [5].

Double Stub Matching

The matching technique presented in the preceding section requires that a reactive element or stub be placed at a precise distance from the load. This point will shift with load impedance. Sometimes it may not be feasible to match the load using a single reactive element. Another possible technique to match the circuit employs two stubs with fixed separation between them. This device can be inserted at a convenient point before the load. The impedance is matched by adjusting the lengths of the two stubs. Of course, it does not provide a universal solution. Separation between the two stubs limits the range of load impedance.

Let ℓ_1 and ℓ_2 be the lengths of two stubs, as shown in Figure 2.6. The first stub is located at a distance ℓ from the load, $Z_L = R + jX$ ohm. Separation between the two stubs is d, and characteristic impedance of every transmission line is Z_0. In double-stub matching, load impedance Z_L is transformed to normalized admittance at the location of the first stub. Since the stub is connected in parallel, its normalized susceptance is added to that and then the resulting normalized admittance is transferred to the location of second stub. Matching conditions at this point require that the real part of this normalized admittance be equal to unity while its imaginary part is canceled by a conjugate susceptance of the second stub. Mathematically,

$$\frac{\overline{Y} + j\left(\overline{B}_1 + \tan(\beta d)\right)}{1 + j\left(\overline{Y} + j\overline{B}_1\right)\tan\left(\beta d\right)} + j\overline{B}_2 = 1 \tag{2.35}$$

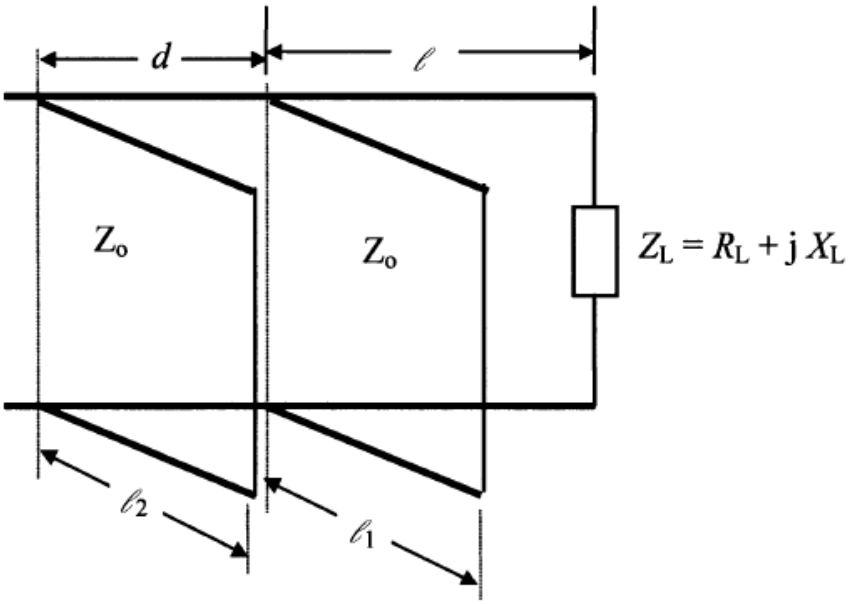

Figure 2.6: Double-stub matching network

where,

$$\overline{Y} = \frac{1 + j\overline{Z}_L \tan\left(\beta\ell\right)}{\overline{Z}_L + j\tan(\beta\ell)} = \frac{\overline{Y}_L + j\tan(\beta\ell)}{1 + j\overline{Y}_L \tan\left(\beta\ell\right)} = \overline{G} + j\overline{B} \tag{2.36}$$

where jB_1 and jB_2 are the susceptance of the first and second stubs, respectively, and β is the propagation constant over the line.

For,

$$\mathrm{Re}\frac{\overline{Y} + j\left(\overline{B}_1 + \tan(\beta d)\right)}{1 + j\left(\overline{Y} + j\overline{B}_1\right)\tan\left(\beta d\right)} = 1 \tag{2.37}$$

$$\overline{G}^2 \tan^2\left(\beta d\right) - \overline{G}\left\{1 + \tan^2(\beta d)\right\} + \left\{1 - \left(\overline{B} + \overline{B}_1\right)\tan(\beta d)\right\}^2 = 0 \tag{2.38}$$

Since conductance of the passive network must be a positive quantity, (2.38) requires that a given double stub can be used for matching only if the following condition is satisfied.

$$0 \le \overline{G} \le \csc^2(\beta d) \tag{2.39}$$

Two possible susceptances of the first stub that can match the load are determined by solving (2.38) as follows.

$$\overline{B}_1 = \cot(\beta d)\left[1 - \overline{B}\tan(\beta d) \pm \sqrt{\overline{G}\sec^2(\beta d) - \{\overline{G}\tan(\beta d)\}^2}\right] \tag{2.40}$$

Normalized susceptance of the second stub is determined from (2.35) as follows:

$$\overline{B}_2 = \frac{\overline{G}^2\tan(\beta d) - \{\overline{B} + \overline{B}_1 + \tan(\beta d)\} \times \{1 - (\overline{B} + \overline{B}_1)\tan(\beta d)\}}{\{\overline{G}\tan(\beta d)\}^2 + \{1 - (\overline{B} + \overline{B}_1)\tan(\beta d)\}^2} \tag{2.41}$$

Once the susceptance of a stub is known, its short-circuit length can be determined easily as follows [6]:

$$\ell_1 = \frac{1}{\beta}\cot^{-1}(-\overline{B}_1) \tag{2.42}$$

and,

$$\ell_2 = \frac{1}{\beta}\cot^{-1}(-\overline{B}_2) \tag{2.43}$$

2.4. LARGE SIGNAL IMPEDANCE MATCHING

Power amplifiers usually employ a matching network between the output transistor and the load. In a class-A stage, if the transistor behaved as an ideal current source, the matching network would simply transform the load resistance to a lower value while presenting no reactive components. In practice, however, the output impedance of the active device is finite, exhibits both real and imaginary parts, and varies with the output voltage and current. Thus, a nonlinear complex output impedance must be matched to a linear load. While we assume herein that the load is resistive and constant, in reality the impedance of the antenna may both contain a reactive component and vary with the position of the transceiver with respect to external objects.

Before dealing with the task of nonlinear impedance matching; first, consider a simple case where the transistor is modeled as an ideal current source with a linear resistive output impedance [Figure 2.7(a)]. An apparent contradiction that occurs here is that the maximum power transfer theorem mandates that $R_L = R_0$, it is required that R_L be transformed to a small value, i.e., typically $R_L << R_0$. Which choice is logical here? If $R_L = R_0$, two problems arise. First, the power delivered to R_L is equal to that dissipated in R_0, reducing the peak efficiency of a class-A amplifier from 50% to 25%. In other words, maximum power transfer does not correspond to maximum efficiency. Second, if R_L is transformed to be as high as R_0, the output power is quite small, the output power is quite small, unless a high supply voltage is used. For these reasons in typical power amplifiers, $R_L << R_0$.

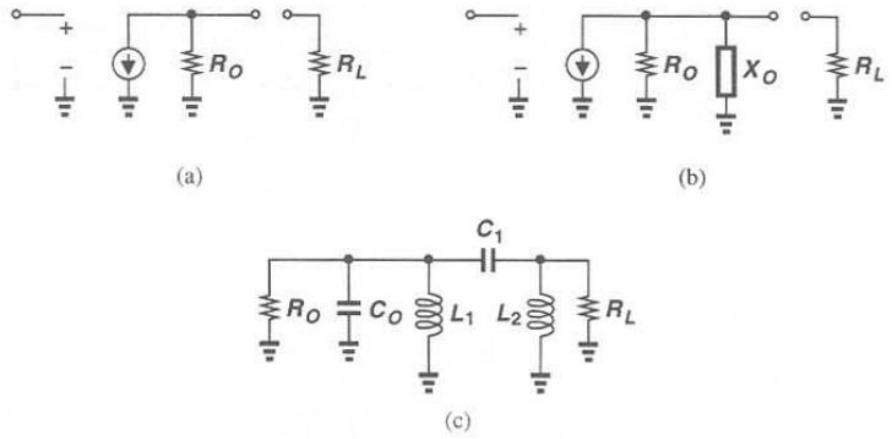

Figure 2.7: Modeling of device output impedance with (a) linear resistance, (b) linear resistance and reactance, (c) simple matching network for (b)

In the next step, suppose, as shown in Figure 2.7(b), the transistor output impedance contains linear real and imaginary parts. Note that since the output transistor is typically several millimeters wide, the magnitude of X_0 at high frequencies is relatively small. The matching network must therefore provide a reactive component to cancel the effect of X_0. Figure 2.7(c) illustrates a simple example where L_1 cancels C_0, and C_1 and L_2 transform R_L while resonating at the fundamental frequency.

Now consider the general case of a nonlinear complex output impedance. A small-signal approximation of the impedance in the midrange of output voltage can be used to obtain rough values for the matching network components, but modifying these values for maximum large-signal efficiency requires a great deal of trial and error, especially if package parasitics must be taken into account. In practice, a more systematic approach called *"load-pull measurement"* is employed.

In a load-pull test, the output power is measured and plotted as a function of the complex load seen by the transistor. Since a complex load requires two axes, the plot actually appears as constant power contours on a complex impedance plane, for

example, a Smith chart. Figure 2.8(a) shows a conceptual setup for load-pull measurement. A variable, precisely calibrated tuner operates as a matching network, presenting various complex impedances to the transistor according to a control input. With the aid of an automated system, the real and imaginary parts of Z_1 are gradually varied such that the power meter maintains a constant reading [Figure 2.8(b)]. In practice, as Z_1 varies so does Z_{in}, necessitating the use of a second tuner between the signal generator and the transistor such that the impedance seen by the generator remains constant (and usually equal to 50Ω).

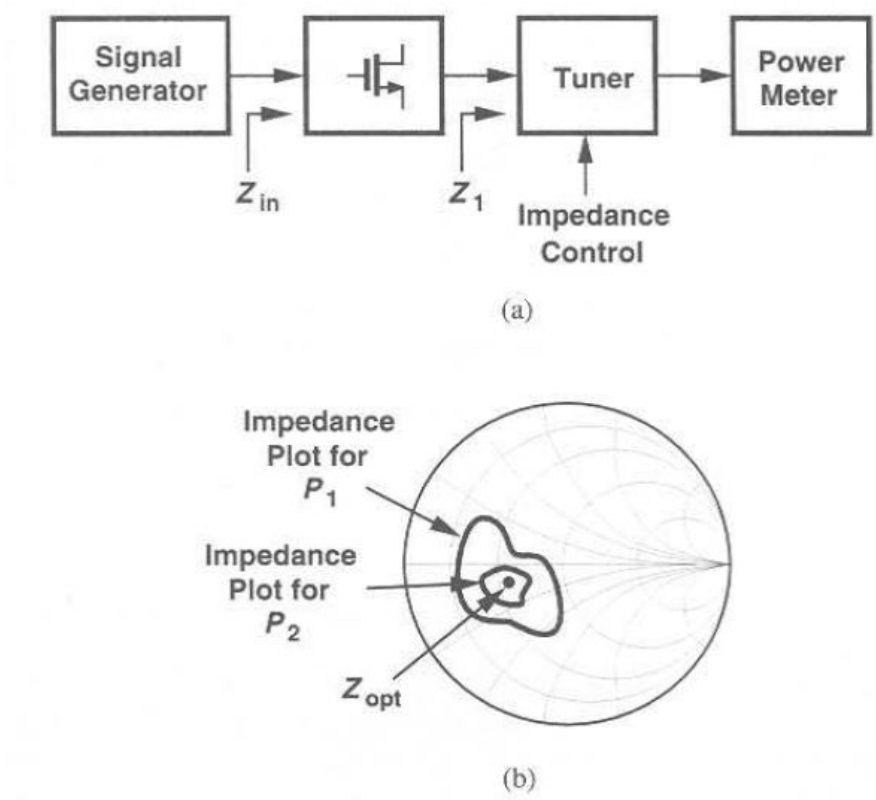

Figure 2.8: (a) Load-pull test, (b) power contours on a Smith chart.

If the power delivered to the input is constant, the output power increases as Z_1 approaches its optimum value, Z_{opt}. This trend is accompanied by a narrower range for Z_1, resulting in tighter contours and eventually a single impedance value,

Z_{opt}, as the output power reaches its maximum level, $P_{\max}$. In other words, the load- pull test systematically narrows down the values of Z_1 so as to obtain both the maximum output power and the corresponding load impedance. Note the power contours also indicate the sensitivity of P_{out} with respect to errors in the choice of Z_1.

The load-pull technique has been widely used in power amplifier design, although it generally requires a computer-controlled setup with extremely precise and stable tuners. This method, however, suffers from three drawbacks. First, the measured results for one device size cannot be directly applied to a different size. Second, the contours and impedance levels are measured at a single frequency and fail to predict the behavior at other frequencies. Third, since the load-pull algorithm does not necessarily provide peaking at higher harmonics, it cannot predict the efficiency and the output power in the presence of multiharmonic termination. For these reasons, power amplifier design using load pull data still entails some trail and error.

In order to avoid complex test setups, the load-pull method can alternatively be implemented in circuit simulation. Similar to the above procedure, the load impedance is varied in small steps and constant power contours are constructed, eventually providing the value of Z_{opt}. Here, too, the procedure is lengthy and cumbersome unless the load variation is automated. Furthermore, such a simulation requires precise modeling of transistors, in particular their output impedance, whereas SPICE models do not accurately represent the output impedance of device at high frequencies and under large variations of voltage and current [7].

2.5. INTERMODULATION DISTORTION & 1-dB COMPRESSION POINT

The electrical noise of a system determines the minimum signal level that it can detect. On the other hand, the signal will be distorted if its level is too high. This occurs because of the nonlinear characteristics of electrical devices such as diodes, transistors, and so on. In this section, distortion characteristics are analyzed.

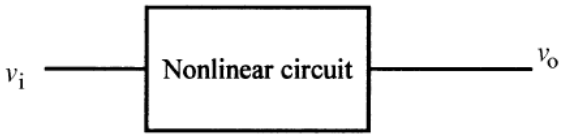

Figure 2.9: Nonlinear circuit with input signal v_i that produces v_o at its output

Consider the nonlinear system illustrated in Figure 2.9. Assume that its nonlinearity is frequency independent and can be represented by the following power series

$$v_o = k_1 v_i + k_2 v_i^{\,2} + k_3 v_i^{\,3} + \ldots \tag{2.44}$$

For simplicity, we assume that the k_i are the real and the first three terms of this series are sufficient to represent its output signal. Further, it is assumed that the input signal has two different frequency components that can be expressed as follows:

$$v_i = a\cos(w_1 t) + b\cos(w_2 t) \tag{2.45}$$

Therefore, the corresponding output signal can be written as

$$\begin{aligned} v_o \approx\ & k_1\left[a\cos(w_1 t)+b\cos(w_2 t)\right]+k_2\left[a\cos(w_1 t)+b\cos(w_2 t)\right]^2 \\ & +k_3\left[a\cos(w_1 t)+b\cos(w_2 t)\right]^3 \end{aligned} \tag{2.46}$$

After simplifying and rearranging it we get

$$\begin{aligned} v_o =\ & k_1\left[a\cos(w_1 t)+b\cos(w_2 t)\right] \\ & +k_2\left[\begin{array}{l} \frac{a^2}{2}\left\{1+\cos(2w_1 t)\right\}+\frac{b^2}{2}\left\{1+\cos(2w_2 t)\right\}+ \\ \quad \frac{ab}{2}\left\{\cos(w1+w2)t+\cos(w_1-w_2)t\right\} \end{array}\right] \\ & +k_3\left[\begin{array}{l} \frac{3}{4}a^3\cos(w_1 t)+\frac{3}{2}ab^2\cos(w_1 t)+\frac{a^3}{4}\cos(3w_1 t)+ \\ \frac{3}{4}ab^2\cos(w_1-2w_2)t+\frac{3}{4}a^2 b\cos(2w_1-w_2)t+ \\ \frac{3}{2}a^2 b\cos(w_2 t)+\frac{3}{4}b^3\cos(w_2 t)+\frac{b^3}{4}\cos(3w_2 t)+ \\ \frac{3}{4}a^2 b\cos(2w_1+w_2)t+\frac{3}{4}ab^2\cos(w_1+2w_2)t \end{array}\right] \end{aligned} \tag{2.47}$$

therefore, the output signal has several frequency components in its spectrum. Amplitudes of various components are listed in Table 2.1.

Figure 2.10 illustrates the input-output characteristics of an amplifier. If input signal is too low then it may be submerged under the noise. Output power rises linearly above the noise as the input is increased. However, it deviates from the linear

Table 2.1: Amplitudes of various harmonics in the output

Harmonic Components	Amplitude
ω_1	$k_1 a + k_3\left(\frac{3}{4}a^3 + \frac{3}{2}ab^2\right)$
ω_2	$k_1 b + k_3\left(\frac{3}{4}b^3 + \frac{3}{2}a^2 b\right)$
$\omega_1 - \omega_2$	$k_2 \frac{ab}{2}$
$\omega_1 + \omega_2$	$k_2 \frac{ab}{2}$
$2\omega_1$	$k_2 \frac{a^2}{2}$
$2\omega_2$	$k_2 \frac{b^2}{2}$
$3\omega_1$	$k_3 \frac{a^3}{4}$
$3\omega_2$	$k_3 \frac{b^3}{4}$
$2\omega_1 - \omega_2$	$\frac{3}{4}k_3 a^2 b$
$\omega_1 - 2\omega_2$	$\frac{3}{4}k_3 ab^2$
$2\omega_1 + \omega_2$	$\frac{3}{4}k_3 a^2 b$
$\omega_1 + 2\omega_2$	$\frac{3}{4}k_3 ab^2$

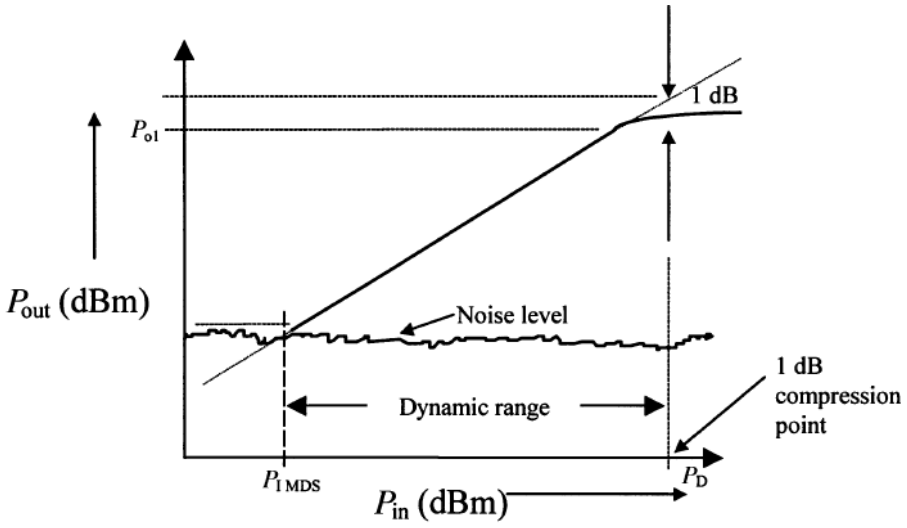

Figure 2.10: Gain characteristics of an amplifier

characteristic after a certain level of input power. In the linear region output power can be expressed in dBm as follows:

$$P_{out}(dBm) = P_{in}(dBm) + G(dB) \tag{2.48}$$

The input power for which output deviates by 1dB below its linear characteristic is known as 1-dB compression point. In this figure, it occurs at an input power of P_D dBm that produces an output of P_{o1} dBm. From the above relation, we find that

$$P_{o1}(dBm) + 1 = P_D(dBm) + G(dB) \tag{2.49}$$

or,

$$P_D(dBm) = P_{o1}(dBm) + 1 - G(dB) \tag{2.50}$$

The difference between the input power at 1-dB compression point and the minimum detectable signal defines the dynamic range (DR). Hence [8],

$$DR = P_D(dBm) - P_{1\,MDS} \tag{2.51}$$

2.6. EFFICIENCY

The drain efficiency is defined as the ratio of RF output power to dc input power, so rises in roughly the same proportion as the fundamental output power if the dc power is constant. The degree of correlation depends on the relative contributions of the harmonics to the total RF output power, and the degree by which the dc input power changes as the device enters saturation. The efficiency is an important parameter in power amplifier design. The power-added efficiency is defined by

$$\eta_{PA} = \frac{(P_{OUT} - P_{IN})}{P_{DC}} \tag{2.52}$$

and measures the incremental RF power added by the device, comparing the output power to the level of input power needed to achieve it. This measure of efficiency depends on the gain of the device since $P_{OUT} = GP_{IN}$. It is a useful performance measure in amplifier design because it tells us the relative contribution and cost made by the device to enhancing power levels [9].

2.7. SUMMARY

This chapter explains non-linear design methods of a broadband power amplifier in theoretically. It is important to understand the theoretical part, because of getting ability to comment the results, and also finding a suitable solution for a problem that is appeared. Design process of power amplifier follows the steps that is seen from the below flow chart.

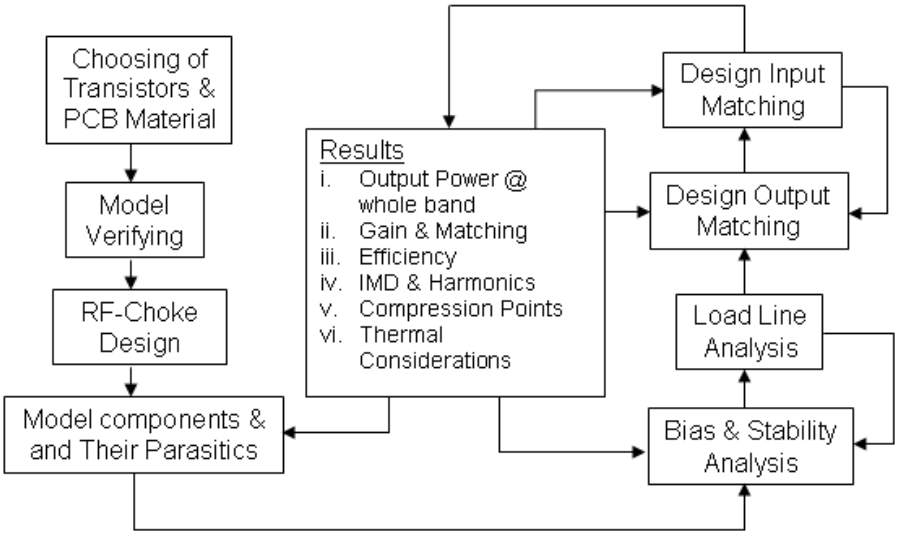

Figure 2.11: Flow chart of the power amplifier design process

As seen from above flow chart, the design is started with choosing of RF power transistor that is used in both the driver stage and the last stage. RF power transistor technology is searched and according to specifications of our design, useful one (Si LDMOS) is chosen. The reasons of choosing this technology will be mentioned at Chapter III. Choosing the printed circuit board material is very crucial because of the operating frequency band of the design. Dielectric constant, loss tangent, and processability of PCB material (i.e. for example through hole plating) are the criterias to make a decision of choosing the suitable PCB material. After choosing the transistors and PCB material, the design process is started.

Initially, RF-Choke is designed, and according to the measurement results, the components and their parasitics are modeled to simulation. Then, biasing and stability, and load line analyses are done sequentially. These analyses are too related to each other; so after analyzing the load line, it is needed to return to analyzing of biasing and stability. Finally, we design the input and output matching network; design of output matching network is done first, then the input matching network is designed, then the output matching network is designed again, as a result the design process of matching networks follows these loop two or three times. Finally we are able to get the simulation and measurement results of the complete power amplifier circuitry. According to measurement results; biasing and stability analysis, designing of input and output matching networks and finally modeling of components and their parasitics are done again. To achieve the best performance at the whole frequency band, these processes are done several times by following the steps that is seen in Figure 2.11.

The design and non-linear modeling process of 500MHz-2GHz power amplifier will be mentioned thoroughly in the following chapters.

CHAPTER III

TRANSISTOR TECHNOLOGIES

There are lost of transistor technologies exist in the market. This chapter gives brief information about transistor technologies that are mostly used. These are the semiconductor technologies:

1. Silicon
    1.1. Silicon CMOS
    1.2. Silicon LDMOS
2. Gallium Arsenide
    2.1. GaAs MESFET
    2.2. GaAs PHEMT
    2.3. GaAs MHEMT
    2.4. GaAs HBT
3. Indium Phosphide
    3.1. InP HEMT
    3.2. InP HBT
4. Silicon carbide
    4.1. SiC MESFET
    4.2. SiC LDMOS
5. SiGe HBT
6. GaN HEMT

3.1. SILICON

Silicon is the most common metalloid. As the eighth most common element in the universe by mass, silicon very rarely occurs as the pure free element in nature, but is more widely distributed in dusts, planetoids and planets as various forms of silicon dioxide (silica) or silicates. On Earth, silicon is the second most abundant element (after oxygen) in the crust, making up 25.7% of the crust by mass.

Silicon has many industrial uses. Elemental silicon is the principal component of most semiconductor devices, most importantly integrated circuits or microchips. Silicon is widely used in semiconductors because it remains a semiconductor at higher temperatures than the semiconductor germanium and because its native oxide is easily grown in a furnace and forms a better semiconductor/dielectric interface than any other material [10].

3.1.1. Silicon CMOS

CMOS provides lower cost advantage. It is capable of producing a small die size because of the small geometries used in advanced CMOS processing. The advantage in total die size offered by CMOS is a function of the ratio of the digital to analog areas of the design. Design with a large digital to analog ratios typically benefits most from the lower geometries of CMOS.

CMOS processes have good linearity across voltage. However, it processes usually do not have the same quality of noise performance as the same sized geometry of other technologies processes [11]**.** CMOS is used in low power amplification processes, especially in cellular phone applications.

Attributes:

- Silicon is so cheap.
- It comes in 12 inch (300 mm) and bigger wafers.
- Processing is cheap. But it is not a good media for microstrip (lossy).
- Silicon by itself doesn't make very good amplifiers above 10 GHz.
- Noise figure and power are all second class to any of the compound semiconductors.
- It can only operate reliably up to 100°C, but silicon is a pretty good heat dissipater [12].

3.1.2. Silicon LDMOS

The recent surge in wireless communication services has created a huge demand for cost-effective, high gain, ultra-linear high power RF transistors for use in base station power amplifiers. Traditionally, RF power transistors have been built using Si bipolar technology, although GaAs power transistors are also available. Recently, laterally diffused metal-oxide-semiconductor (LDMOS) transistors have been proven to be very popular for these applications. They have superior RF performance compared to bipolar transistors and are highly cost-effective compared to their GaAs counterparts.

The cross-section of a typical LDMOS transistor is shown in Figure 3.1 The device has a high doped p-type sinker diffusion, used to ground the Source to the substrate. This eliminates the need for an external connection from Source to the ground, and hence minimum common lead inductance and maximum RF gain. The p-type body region under the Gate forms the channel. Devices have been fabricated to operate from 3 volts up to 48 volts on the Drain. Higher breakdown voltages are accomplished in LDMOS devices by the Lightly Doped Drain (LDD) region, also called the drift region. In absence of the LDD region, most of the applied voltage

appears across Gate oxide and leads to breakdown by impact generation in the substrate region. This results in a specific breakdown voltage for a given oxide thickness. Hence, the Drain is receded away from the Gate by formation of an LDD region between the Gate and Drain edges. The LDD is carefully designed to support a uniform electric field during breakdown. Figure 3.2 shows the path for current flow in the transistor when a Gate bias higher than threshold voltage is applied. It can be noticed that the current flow is in a lateral direction and there is no significant current crowding in the channel region.

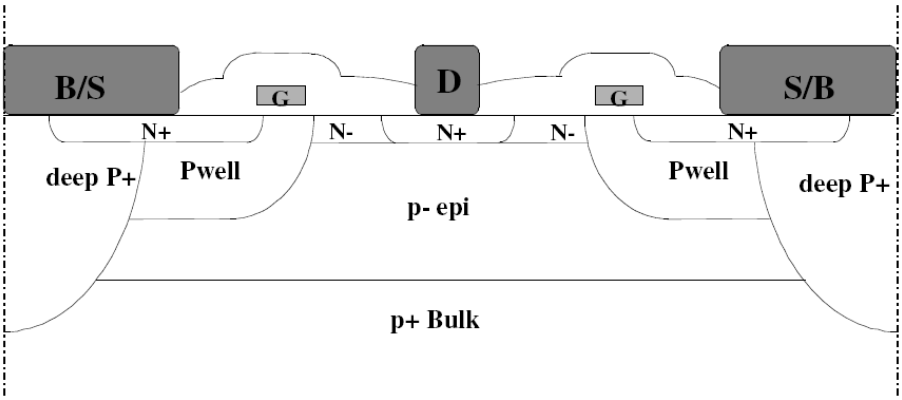

Figure 3.1: Cross section of an LDMOS transistor

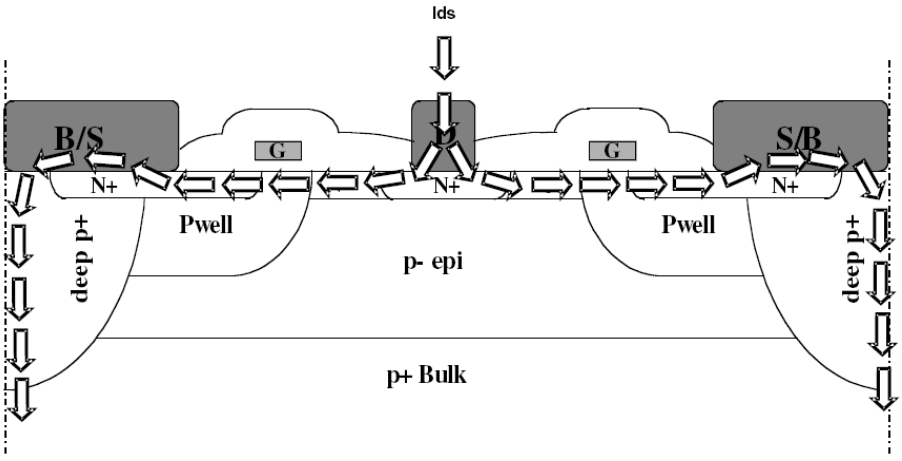

Figure 3.2: Current path in an LDMOS transistor ($V_{GS} > V_{th}$)

LDMOS transistors have a major advantage compared to bipolar transistors because of their “immunity” to thermal runaway. An increase in die temperature causes an increase in the Source resistance and hence reduced current flow [13].

Although some vendors offer RF versions of DMOS, its vertical structure has serious problems with excessive parasitic capacitance starting at around 500 MHz. LDMOS fares much better at higher frequencies, not least due to extensive technology development recent years. LDMOS components with output power over 100 Watts at 2.7 GHz are available at the moment.

High power LDMOS devices typically provide internal impedance matching for intended frequency band. The practical power limit for LDMOS without internal matching is around 10 Watts at 2.5 GHz. This might leave a window of opportunity for other materials in broadband power designs. Wide bandgap materials offer higher output power per 1pF of gate capacitance, which is an advantage for broadband applications.

What is so special with LDMOS? As a device of MOSFET variety, LDMOS uses an inversion channel at the silicon-oxide interface. The inversion channel is induced under the gate by positive gate potential. Under practically relevant conditions the inversion layer only exists over the laterally diffused P-well, which is sometimes called depletion stopper. As the electrons leave the region over the stopper they are picked up by the electric field due to positive drain bias and abandon the inversion channel going deeper into the bulk. The effective gate length defines the lateral extension of the stopper layer. It may be therefore shorter than the physical length of the gate electrode.

High breakdown voltage of LDMOS is one of its most important advantages. For a given output impedance the power output is the square of voltage swing, therefore

you get over 7dB more power going from 12V to 28V V_{dd}. Even if you are able to match that low-voltage component you will lose some bandwidth and you will certainly need a lot of current out of your power supply. So why does LDMOS have higher operation voltage than silicon than GaAs MESFET if the breakdown field in GaAs is higher than in silicon? Examination of the cross-sections will give the answer to this question. Electric field crowding at the gate edge of the MESFET takes up all the advantages of the higher breakdown field of GaAs. In addition, the current pathway through the buffer layer does not offer the designer much choice apart from increasing the gate length to make a tradeoff between gain and output power. In LDMOS the depletion stopper and the field plate form a fairly uniform electric field between gate and drain. Electric field crowding at the apparently sharp edge of the field plate has little effect on the breakdown in LDMOS, since the breakdown field of the oxide is much more over than that of silicon [14].

Table 3.1 summarizes the features of an LDMOS transistor that make it the technology of choice for present-day high power linear amplifiers [15], and Table 3.2 shows the features of some of the transistor technologies in comparison.

Table 3.1: Features of LDMOS Transistors

Attribute	Effective Parameter	Benefit
Higher gain	High G_m and low C_{rss}	Lower system cost due to fewer stages. Increased gain can be traded for enhanced stability.
Higher efficiency	Low $R_{DS(on)}$ and low C_{oss}	Lower junction temperature for same output power, hence greater system performance and higher MTBF.
Greater stability	Low C_{rss} and very low Source inductance	Easier design.
Simplicity of use	High input resistance, single supply, and backside Source contact	Very little Gate current, hence simple Gate bias circuits. Dual supply sources not needed.
Improved linearity	$I_{D(sat)}$ and G_m flatness	Less output distortion, reduced overall system power for the same degree of linearity.

Table 3.2: Features of different transistor technologies

	MESFET/HEMT	III-V HBT	Si BJT	Si:Ge HBT	Power MOSFET (LDMOS)
			Low Voltage Related Characteristics		
Parasitic loss	Very good	Very good	Moderate	Moderate	Moderate
Single-polarity supply	No	Yes	Yes	Yes	Yes
Power added efficiency	Excellent	Very good	Moderater	Moderate	Good for f<~2 GHz
Linearity	Excellent	Very good	Moderate	Very good	Moderate
Power density	Moderate	Excellent	Very good	Excellent	Moderate
			General Characteristics		
Cost	Moderate to high	Moderate to high	Low to moderate	Moderate to high	Low to moderate
Maturity	Good	Good	Excellent	Moderate	Very good

3.2. GALLIUM ARSENIDE (GaAs)

Engineers estimate that within the next 10 to 15 years we will reach the limit, in terms of size and performance, of the silicon transistors key to the industry. As a result, they are working on new materials and technologies that may be able to reach beyond the limits of silicon. One such material is investigated a family of semiconductors known as III-V compound semiconductors. Unlike silicon, these are composite materials. A particularly hot prospect is indium gallium arsenide, or InGaAs, a material in which electrons travel many times faster than in silicon. As a result, it should be possible to make very small transistors that can switch and process information very quickly. It is demonstrated by fabricating InGaAs transistors that can carry 2.5 times more current than state of the art silicon devices. More current is the key to faster operation [16].

Gallium arsenide (GaAs) is a compound of two elements, gallium and arsenic. It is an important semiconductor and is used to make devices such as microwave frequency integrated circuits (i.e., MMICs), infrared light-emitting diodes, laser diodes and solar cells.

GaAs has some electronic properties which are superior to those of silicon.

- It has a higher saturated electron velocity and higher electron mobility, allowing transistors made from it to function at frequencies in excess of 250 GHz.
- Also, GaAs devices generate less noise than silicon devices when operated at high frequencies.
- They can also be operated at higher power levels than the equivalent silicon device because they have higher breakdown voltages.

These properties recommend GaAs circuitry in mobile phones, satellite communications, microwave point-to-point links, and some radar systems. It is used in the manufacture of Gunn diodes for generation of microwaves.

Another advantage of GaAs is that it has a direct bandgap, which means that it can be used to emit light efficiently. Silicon has an indirect bandgap and so is very poor at emitting light. (Nonetheless, recent advances may make silicon LEDs and lasers possible).

Silicon has three major advantages over GaAs for integrated circuit manufacture.

1. First, silicon is abundant and cheap to process. Si is highly abundant in the Earth's crust, in the form of silicate minerals. The economy of scale available to the silicon industry has also reduced the adoption of GaAs.
2. The second major advantage of Si is the existence of silicon dioxide (one of the best insulators). Silicon dioxide can easily be incorporated onto silicon circuits, and such layers are adherent to the underlying Si. GaAs does not form a stable adherent insulating layer.

3. The third, and perhaps most important, advantage of silicon is that it possesses a much higher hole mobility. This high mobility allows the fabrication of higher-speed P-channel field effect transistors, which are required for CMOS logic. Because they lack a fast CMOS structure, GaAs logic circuits have much higher power consumption, which has made them unable to compete with silicon logic circuits [17].

In the latest research, the researchers have improved the stability and electrical characteristics of the gate oxide, comprised of gallium oxide and gadolinium oxide. As a result, the current decreases only 1.5 percent after 150 hours of operation under extreme conditions. In contrast, the previously best research results reported a 22 percent drop over a three-hour period.

Currently, most wireless applications use gallium arsenide metal-semiconductor field-effect transistors (MESFETs), which lack a gate oxide, but which are necessary because higher frequencies are attainable with gallium arsenide compared to silicon. (That's because electrons can travel five to six times faster in gallium arsenide-based transistors.)

Because of the lower power consumption of gallium arsenide MOSFETs, the talk time for cellular phones would be extended. Meanwhile, wireless base stations would be more powerful and more efficient [18].

3.2.1. GaAs MESFET

Gallium arsenide MESFET is the original answer to "how can we make amplifiers at microwave frequencies?". The first GaAs MMICs demonstrated in the 1970s. Including HEMT and HBT technologies, literally billions of dollars have been spent extending of GaAs products up into hundreds of GHz.

Attributes:

- The semi-insulating properties of GaAs substrates and the 12.9 dielectric constant make it an excellent media for microstrip.
- It operates reliably up to channel temperature.
- GaAs substrates are available up to six inches (150 mm) in diameter, which has been a long development since the first 2-inch wafers were available in the late 1970s.
- Sadly, GaAs MESFET MMICs will never be cheaper than silicon, due to the starting material cost ($100s of dollars).
- GaAs parts are more fragile than silicon, and the thermal dissipation factor is not that good.
- GaAs MESFETs may be extinct in five years, because it doesn't cost much more to fabricate PHEMT or MHEMT on GaAs, and these technologies offer higher performance [12].

Table 3.3: Advantages and disadvantages of GaAs MESFET transistor technology

Advantages	Disadvantages
• Mature technology • Optical gates (usually) means low cost • Great microwave substrate (12.9 ε_r, low loss tangent, high bulk resistivity) • Six inch wafers available • Photonic properties • 16-20 V breakdown possible • Relatively cheap to produce (but always more than silicon) • Channel temperatures up to 150ºC possible	• Limited to 18GHz or lower • Noise figure and power performance not as good as GaAs PHEMT • Positive and negative voltage typically needed (V_{GS} and V_{DS}).

3.2.2. GaAs PHEMT

GaAs PHEMT was the second MMIC technology to be perfected, in the 1990s. Breakdown voltages of PHEMT up to 16 volts make high power and high efficiency amplifiers possible, and noise figure of tenths of dB at up to 12 GHz means great LNAs.

PHEMT stands for pseudomorphic high electron mobility transistor. "Pseudomorphic" implies that the semiconductor is not just GaAs, perhaps AlGaAs/InGaAs/GaAs.

Actually, "pseudomorphic" means that the hetero layers are thin enough not to keep their own crystal lattice structure, but assume the structure (lattice constants especially) of surrounding material (lots of stress is involved). For a GaAs pHEMT, indium is added to improve mobility and form a quantum well. Indium wants to growth the lattice and the typical range for useful thicknesses would be 10-25% on GaAs. It can be also done strain compensation with the Schottky or cap layer [12].

Table 3.4: Advantages and disadvantages of GaAs PHEMT transistor technology

Advantages	Disadvantages
• Useful through 40-52GHz, especially if thinned to 2 mils and individual source vias are used • Excellent power and efficiency (greater than 60% PAE) • Breakdown 12 volts at best, typical operate at 5-6 volts • Channel temperatures up to 150°C possible.	• E-beam gates (increases cost) • Positive and negative voltage typically needed (V_{GS} and V_{DS})

3.2.3. GaAs MHEMT

Recent work on metamorphic MHEMT has made premium InP HEMT performance possible (amplifiers up at 100 GHz) at the same price as "regular" GaAs PHEMT. Noise figure and equal to indium phosphide by using MHEMT, reputable foundry and indium content is high. It is actually possible to exceed InP RF performance with indium content greater than 55%. The down side to all that indium is reduced operating voltage.

MHEMT stands for metamorphic high-electron mobility transistor. The channel material is InGaAs. "Metamorphic" implies that the lattice structure of GaAs is buffered using epitaxial layers to gradually transform the lattice constant so it lines up with InGaAs. InGaAs is normally grown on InP, which is expensive and fragile compared to GaAs. "Metamorphic" is changing the lattice constant by bond breaking as opposed to "pseudomorphic" [12].

Table 3.5: Advantages and disadvantages of GaAs MHEMT transistor technology

Advantages	Disadvantages
• Extremely low noise figure • Incredibly high operating frequency (more than 100 GHz) • Extremely low on-resistance makes great switches, but not as well as PIN diodes. • Channel temperatures up to 150°C possible.	• Breakdown voltage much lower than PHEMT • Low operating voltage (1 to 2 volts) • Positive and negative voltage typically needed (V_{GS} and V_{DS})

3.2.4. GaAs HBT

The heterojunction bipolar transistor (HBT) is a new development, and can decrease the cost of GaAs amplifier products because the emitters are formed optically. GaAs HBT devices operate vertically, compared to the horizontal operation of FETs. However, for very high frequency, the emitter size must be made quite small, and the InGaAs layer is thick and is a thermal insulator, so these devices tend to run hot. Typical HBT amplifiers are "gain blocks", used in the UHF to 8GHz frequency ranges [12].

Table 3.6: Advantages and disadvantages of GaAs HBT transistor technology

Advantages	Disadvantages
• Single power supply polarity • All-optical process	• Heat dissipation can be problem at small emitter size • Typically, reverse isolation is not as high as with PHEMT amplifiers, leading to poor amplifier directivity. • Collector resistors are required to stabilize amplifiers. These cut into the power efficiency.

3.3. INDIUM PHOSPHIDE

3.3.1. Indium Phosphide HEMT

Indium phosphide HEMT has broken all of the upper frequency records, on the way to terahertz devices. However, there are serious drawbacks to this technology, not the least of which is its high cost. For this reason, InP is more regarded as a lab curiosity rather than a production process.

The actual semiconductor that is doing the work in so called InP is actually InGaAs. Indium phosphide is merely the substrate that it is grown onto. The reason for this is that InGaAs shares the same lattice constant with InP, 5.87 angstroms.

Attributes:

- InP substrates are small (3" typical, 4" are available but remember bigger is not always better when something is brittle).

- ε_r=12.4, close to that of GaAs.
- A huge drawback of indium phosphide technology is that InP wafers are extremely brittle compared to other semiconductors [12].

Table 3.7: Advantages and disadvantages of InP HEMT transistor technology

Advantages	Disadvantages
• Extremely low noise figure • Useful through W-band and beyond	• More expensive than GaAs due to starting material costs, small size of wafers. • Extremely fragile. • Low breakdown voltage (power is low)

3.3.2. Indium Phosphide HBT

Some people think that InP will have a second chance to become the most ubiquitous power amplifier technology for cell phones when new higher power density/lower voltage lithium ion batteries become available. InP has superior low voltage performance compared to GaAs HBT [12].

3.4. SILICON CARBIDE (SiC)

Silicon carbide (SiC) is a compound of silicon and carbon bonded together to form ceramics, but it also occurs in nature as the extremely rare mineral moissanite. Pure α-SiC is an intrinsic semiconductor with bandgaps of 3.03eV-3.28eV respectively. Historically, it was used in early radio as a detector.

Silicon carbide is used for blue LEDs, ultra fast, high voltage Schottky diodes, MOSFETs and high temperature thyristors for high-power switching. Currently, problems with the interface of SiC with silicon dioxide have hampered the development of SiC based power MOSFET. Another problem is that SiC itself breaks down at high electric fields due to the formation of extended stacking faults, but this problem may have been resolved relatively recently.

Due to its high thermal conductivity, SiC is also used as substrate for other semiconductor materials such as gallium nitride. Due to its wide bandgap, SiC-based parts are capable of operating at high temperature (over 350°C), which together with good thermal conductivity of SiC makes SiC devices good candidates for elevated temperature applications. SiC devices also possess increased tolerance to radiation damage, making SiC a desirable material for defense and aerospace applications. Gallium nitride is itself also an alternative material in many applications. Although diamond has an even higher bandgap, SiC-based devices are easier to manufacture because is more convenient to grow an insulating layer of silicon dioxide on the surface of a silicon carbide wafer than it is on diamond.

Pure SiC is a poor electrical conductor. Addition of suitable dopants significantly enhances its conductivity. Typically, such material has a negative temperature coefficient between room temperature and about 900°C, and positive temperature coefficient at higher temperatures, making it suitable material for high temperature heating elements [19].Active silicon transistors reach their normal operational temperature limits at approximately 125°C, typically have a switching limit in the range of a few GHz, and are highly susceptible to harsh environments (most notably, intense radiation and thermal environments). SiC devices have the potential to operate at temperatures up to 600°C at switching frequencies in the 10s to 100s GHz range and at increased power densities, thus improving upon many of the limitations associated with silicon electronics.

Silicon carbide (SiC) is a semiconductor material with desirable properties for many applications. These desirable properties are primarily due to its wide energy bandgap, a property of semiconductors that determines the amount of energy needed to make the material carry current. Due to this wide bandgap (3.0-3.3 electron volts), heat and other external influences do not readily disrupt the performance of SiC microelectronics. Therefore, SiC devices can operate at higher temperatures and higher radiation levels than silicon and gallium arsenide based devices. SiC can also operate at higher power levels, and it can emit blue light. Some other desirable properties of SiC include a high maximum electron velocity (which means that SiC devices can operate at high frequencies), a high thermal conductivity (which means that SiC devices can easily dissipate excess heat), and a high breakdown electric field (which means that SiC devices can operate at high voltage levels) [20].

Extend these possibilities to a longer-term outlook, and the future for SiC becomes even brighter. Thermal issues are some of the most problematic concerns associated with today's computer systems. In fact, these are the driving issues in transferring technology from the desktop system to the laptop. Imagine the reduction in the size of commercial electronics if transistor junction temperatures can operate at 400°C or 600°C instead of today's silicon electronics' limit of 125°C (or in the case of commercial electronics, typically 80°C). Another future industry undoubtedly will be the automobile industry, regardless of whether it's gasoline or electric driven. In the case of electric or hybrid-electric vehicles, all of the advantages associated with the military's hybrid-electric combat vehicles would be directly applicable to domestic vehicles. In the case of gasoline engines, SiC IC technology would become important. Currently, automobile electronics have to be shielded within the engine compartment (or kept away from the engine compartment) due to the thermal issues. SiC would remove that problem, allowing sensor and control electronics to be mounted directly on or in the engine block, thus improving automobile efficiency and performance [21].

3.4.1. Silicon Carbide MESFET

Features of wide bandgap semiconductors that provide high RF power density, excellent power added efficiency (PAE) performance, high breakdown voltage, high-frequency operation, small die size, and less complex amplifier arrangement make such technology a serious challenge to silicon LDMOS devices for high-power applications. Over the last years, many authors have utilized these superior features of SiC MESFETs and have applied them in the development of different generations of power amplifiers for use in digital audio and video broadcasting and aerospace and military systems.

A comparison of Si, GaAs and SiC MESFET power densities indicates that SiC is a very promising material for high power and high frequency operation. A serious problem of wide band power amplifiers, especially in the GaAs field effect transistor (FET) and GaAs monolithic microwave integrated-circuit (MMIC) cases is the output matching because of the low intrinsic device impedance. Depending on the amplifier data, this problem can be mostly overcame only by using (external) transmission line transformers that strongly limit the total bandwidth. The SiC-MESFET technology avoids this drawback and provides high large signal output impedance because of its high drain-source breakdown voltage. In hybrid arrangements, the advantages of GaAs and SiC can be combined successfully [22].

3.4.2. Silicon Carbide LDMOS

Laterally diffused metal oxide semiconductor technology, used to make power amplifiers. It can withstand 200°C channel temperatures and it is good to 3 GHz, and 10W output power [12].

3.5. Silicon Germanium HBT

SiGe is a new development (in the last five years), and was originally predicted to put all forms of GaAs into the history books. SiGe can make very cheap parts, with performance maybe into millimeter wave, and processing on eight-inch (200 mm) diameters wafers. But the devices are not as high performance as GaAs, in terms of noise figure and power.

Every time the upper frequency of SiGe extended, the breakdown voltage is reduced. Some of that stuff has to operate at 1.0 volts [12].

Table 3.8: Advantages and disadvantages of SiGe HBT transistor technology

Advantages	Disadvantages
• Eight inch silicon wafers mean low production cost in high volume • All-optical process (also low cost) • Possible to add scads of logic onto RF chip (BiCMOS logic)	• Low V_{br}, as bad as 1.5 volts • Electrically, Si is not a great insulator • Thermal runaway? • 110°C max junction temperature • No equivalent of a switch FET, so phase shifters and attenuators are a problem • Not many foundries do SiGe • High setup charges due to expensive mask set

3.6. GaN HEMT

This is the future of microwave power amplifiers; GaAs has exceeded its half life. It's more expensive than other technologies. GaN offers a path to much higher power densities and therefore cheaper costs per Watt. Breakdown voltages of 100 Volts are possible; soon you will be able to buy 48 volt solid state power amps at X-band. GaN is still a relatively immature process; reliability has been a huge problem that is just being overcome. Ancillary stuff like higher voltage capacitors and resistors, and backside processes need to be redeveloped at MMIC foundries in order to participate in this new technology.

Substrates for GaN are silicon carbide, sapphire, or silicon. Native GaN wafers are impractical, so a lot of expensive alchemy is needed to align the GaN crystal onto mismatched substrates. Four-inch SiC substrates are just becoming available, for GaN-on-silicon, four inch wafers are also available.

SiC is an excellent heat sink and GaN can operate up to greater than 150°C channel temperature. Below 2GHz, expect to see GaN used in base station applications, competing with silicon carbide technology. Higher frequency GaN products will be fielded by the military.

Silicon is not such a great heat sink as silicon carbide (40 versus 350 W/m-K), so lower cost of GaN on silicon may be outweighed by the ability to dissipate higher power (and thereby achieve greater power density) on SiC Normally, silicon's conductivity makes it lossy as an RF substrate [12].

Table 3.9: Advantages and disadvantages of GaN HEMT transistor technology

Advantages	Disadvantages
• Up to 10 times the power density of GaAs PHEMT has been demonstrated. • Higher operating voltage, less current. • Excellent efficiency possible. • Can operate hotter than GaAs, Si or SiGe.	• Expensive • Reliability not established yet • You have to deal with a huge heat flux.

CHAPTER IV

SINGLE STAGE DESIGN OF MW6S004NT1 TRANSISTOR

4.1. INTRODUCTION

This section presents modeling and analysis of the driver stage of 500MHz-2000MHz broadband power amplifier. The design is tried to model in simulation when high level signal is given as an input, so we are able to model non-linear characteristic of the amplifier.

Kinds of printed circuit boards are searched thoroughly and most suitable one of Rogers Company's RO4000 Series High Frequency Circuits Materials of RO4003C is chosen. Table 4.1 compares the features of PCBs such as Isola Company's FR402, Rogers Company's RO4003C, and Rogers Company's RT/duroid 5880.

Table 4.1: Comparison of the PCB materials

Materials / Features	Isola FR4	Rogers RO4003C	Rogers RT/duroid 5880
Dielectric Constant	4.25 (@1GHz)	3.38 (@10GHz)	2.20 (@10GHz)
Dissipation Factor (Loss Tangent)	0.015 (@1GHz)	0.0021 (@2.5GHz)	0.0009 (@10GHz)
Thermal Conductivity (W/m/K)	0.36	0.64	0.2
Processabilty (Through Hole Plating)	√	√	X

As seen from the above table, Isola FR4 material has the higher dielectric constant and dissipation factor, so this material cannot be used for application of 500MHz-2GHz frequency band. On the other hand, Rogers RT/duroid 5880 isn't a processable material for our PCB processing infrastructure. So, we choose the best alternative of PCB material which is Rogers RO4003C. Besides, thermal conductivity feature of any PCB material is very important for power amplifier design. As seen from Table 4.1, Rogers RO4003C has the best thermal conductivity feature, so this is suitable for cooling the whole system.

Initially, we start to design this amplifier with simulations using Advanced Design System 2008 Update 2. Large signal model of MW6S004NT1 transistor is obtained from Freescale Company.

For the last stage, we decide to use NXP Company's BLF3G21-6 transistor. This transistor has 6W output power. Although there are some LDMOS transistors that provide more output power than BLF3G21-6, they don't have large signal model so

we aren't able to make Harmonic Balance Simulation of the amplifier. Harmonic Balance method will be explained thoroughly in appendix part. Consequently, using a transistor which doesn't have large signal model is not suitable for this thesis's purpose. Because of this reason, we choose BLF3G21-6 transistor that obtains the highest output power and also has large signal model. I will mention this in next chapter.

In single stage design process, the configuration that showed in Figure 4.1 is used.

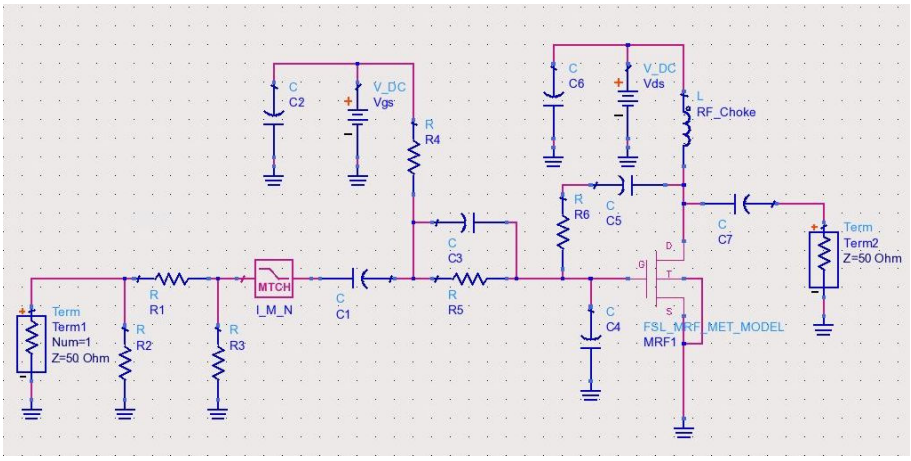

Figure 4.1: Schematic of single stage configuration

For stability of the transistor, series resistor (R5), shunt resistor (R4), and feedback resistor (R6) are optimized. PI attenuator and matching network are used to match the transistor input impedance (to decrease the input return loss) to 50ohm. RF Choke is used to isolate the RF transmission line from the DC source. It is important that RF Choke has a feature that can support to pass enough DC current through the transistor. I will deeply mention the design processes in the following sections.

As seen in Figure 4.2, there is no output matching network used at the output of the single stage configuration. Because, MW6S004NT1 transistor's output impedance is quite matched to BLF3G21-6 transistor's input impedance. In simulations, we see that there is no need to put an inter stage matching network between them. So we directly connect the driver stage output to input of the last stage.

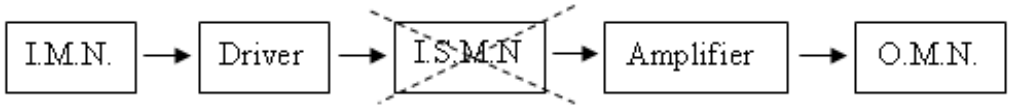

Figure 4.2: General configuration of two stage power amplifier

I.M.N.	: Input Matching Network
Driver Stage	: Freescale MW6S004NT1
I.S.M.N	: Inter Stage Matching Network
Last Stage	: NXP BLF3G21-6
O.M.N.	: Output Matching Network

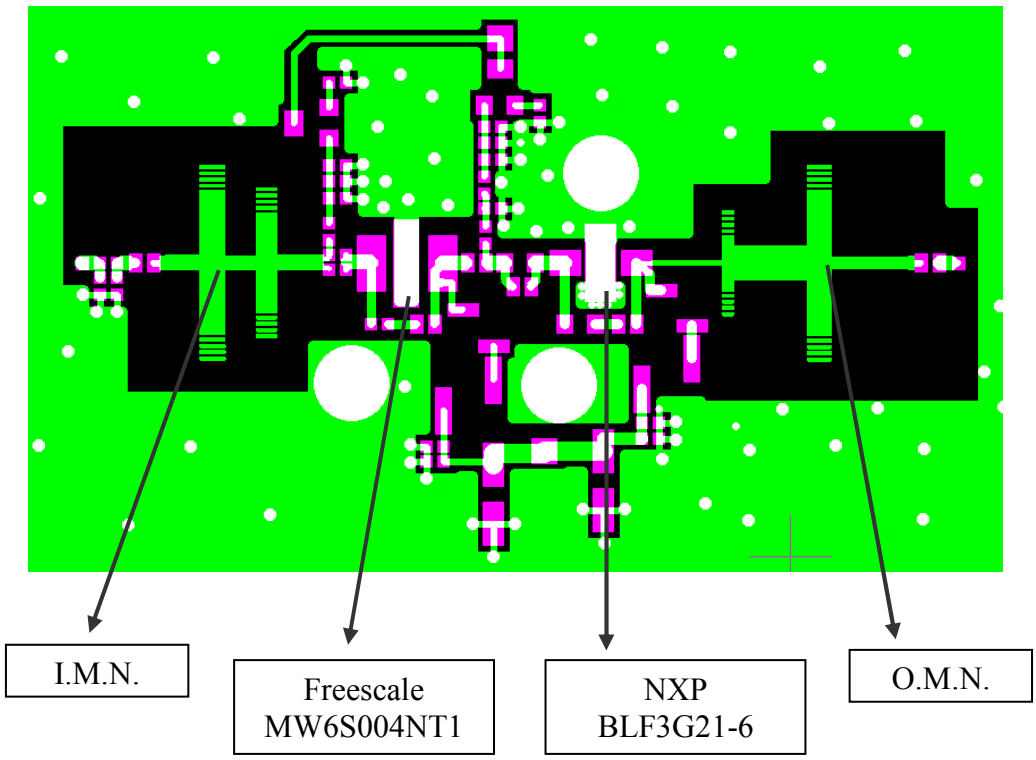

Figure 4.3: Layout of the overall system on PCB

Microstrip lines and open circuit stubs are used in the input and the output matching networks. The length and width values of microstrip lines and open circuit stubs are found from simulations. Furthermore, 2dB PI type attenuator is used at the input section to improve input return loss; on the other hand, stability of the driver stage gets better after putting 2dB attenuator at the input section.

Measurement process begins with analyzing of driver stage, and then it continued with analyzing of last stage. The input impedance of driver stage is tried to match to 50 ohm termination by using an input matching network, but the output impedance of driver stage isn't tried to matched to 50 ohm, because we don't make any 50 ohm matching networks between the driver and the last stages. So, when we design the driver stage by individually, the output return loss is found to be worse, as expected. As a result, this causes to get some measurement results worse. In the multistage

configuration, there is not 50 ohm termination point at the output of the driver stage, so driver stage sees the input impedance of the last stage. Analyzing the driver stage by separating from the last stage causes these results, but these results will not produce any problem for the system, because when the output of the driver stage directly sees the input impedance of the last stage, it is time to get the real results.

In the single stage configuration, after getting measurement results we try to model the lumped components and their parasitic effects in simulation. We see that measured and simulated results are so close to each other; the modeling process is done successfully.

4.2. CRITERIAS OF CHOSING FREESCALE MW6S004NT1 TRANSISTOR

RF power transistor of MW6S004NT1 that is developed by Freescale Company has LDMOS (Laterally Diffused Metal-Oxide-Semiconductor) technology. Although the criterias of choosing LDMOS technology are mentioned at previous section, if we want to remind them, LDMOS technology;

a. is suitable for our frequency band.
b. doesn't have any reliability problem.
c. doesn't have any stability problem. Stability at broadband can be obtained by RF feedback components.
d. has high gain at broadband.
e. is suitable for efficient working.
f. has adequate linearity.
g. is cheaper than the other technologies (GaAs, GaN, SiC / HEMT, PHEMT, MESFET).

From these features, it seems that LDMOS technology is sufficient for our design. Although there are some specific advantages for GaAs, GaN or SiC transistor technology over Si LDMOS transistors;

- input and output impedances are not as scattered as LDMOS's
- works more efficiently
- has higher linearity characteristics,
- can work at broader frequency band

costs of them are many times more over LDMOS's, so we decide to choose Silicon LDMOS technology for our design.

MW6S004NT1 transistor is produced by Freescale Company. If we look at the transistor data sheet, we can see that it might be used in our design.

According to the transistor's data sheet;

i. frequency band: 1MHz - 2000MHz
ii. maximum output power: 4W
iii. Power gain: 18 dB (@Pout = 4W)
iv. Drain efficiency: 33% (@Pout = 4W)
v. IMD: -34 dBc (@Pout = 4W)

MW6S004NT1 has these features. From these features, it seems that this transistor can be used at driver stage in the two stage amplifier configuration.

4.3. SIMULATIONS & MEASUREMENTS

4.3.1. DC BIASING

MW6S004NT1 transistor works with 28V. It is important to determine I_{dq} value of the transistor to get a load line that makes an optimum swing at $I_{dq} - V_{gs}$ graph at 27dBm output power. In simulation, we see that 80mA is enough for class-A operation to get 27dBm output power at the whole band.

The graphs below show the load lines of the single stage system at Pout=27dBm where the frequency of input signal frequency is at 500MHz, 1000MHz, 1500MHz, and 2000MHz.

For 500MHz input signal:

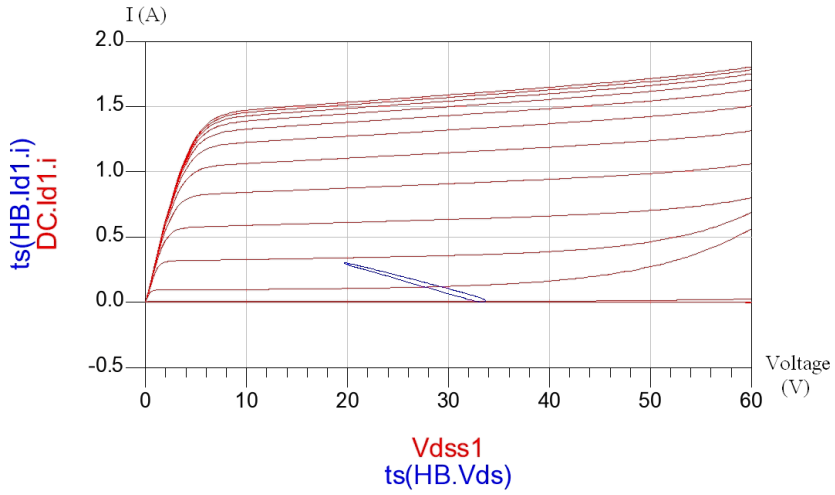

Figure 4.4: Load line in simulation at $f_c = 500MHz$ for single stage configuration

For 1000MHz input signal:

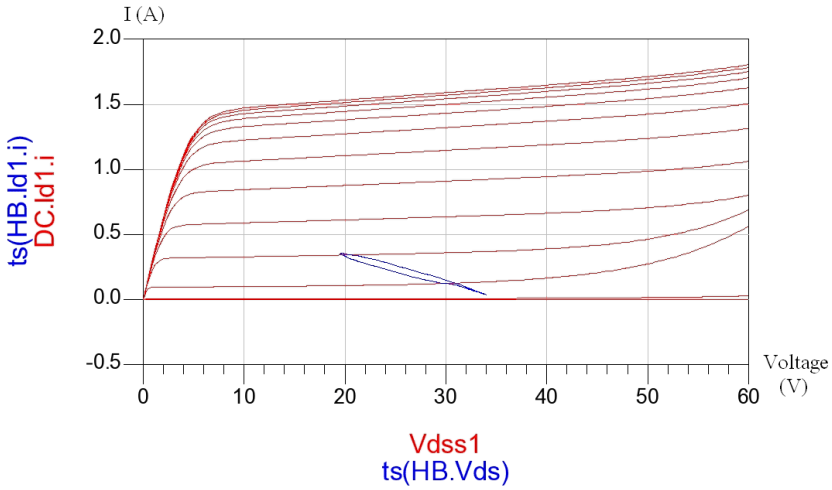

Figure 4.5: Load line in simulation at $f_c = 1000MHz$

for single stage configuration

For 1500MHz input signal:

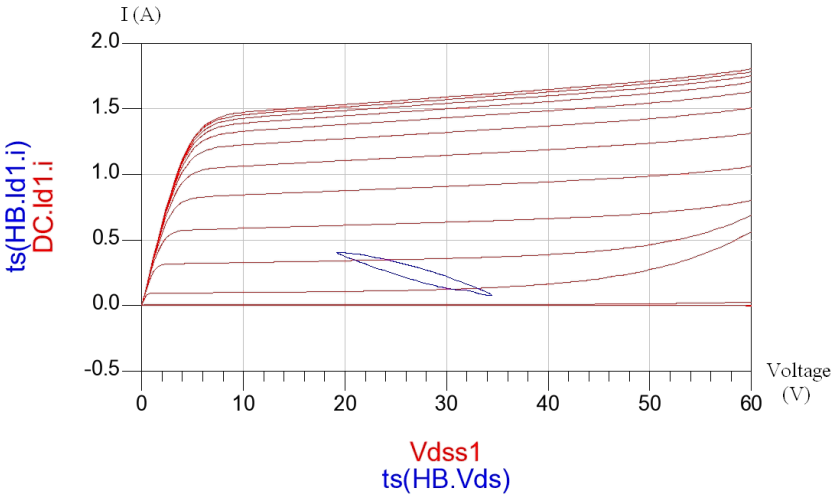

Figure 4.6: Load line in simulation at $f_c = 1500MHz$

for single stage configuration

For 2000MHz input signal:

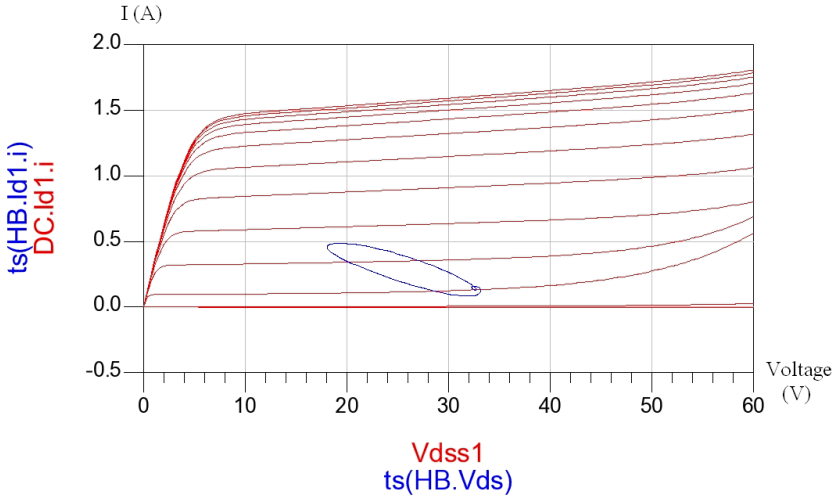

Figure 4.7: Load line in simulation at $f_c = 2000MHz$ for single stage configuration

From the above figures it can be seen that the load line is getting an elliptic shape at higher frequencies, because of capacitive effect at the output of the transistor. This will probably cause to reduce the efficiency of the driver stage at higher frequencies.

4.3.2. DC BIASING NETWORK (DESIGN OF CHOKE)

Designing a RF-choke is very crucial in broadband amplifier design. The importance of RF-choke comes from being able to support the required DC source to the transistor, and isolate the RF transmission line from the DC source line at the whole band.

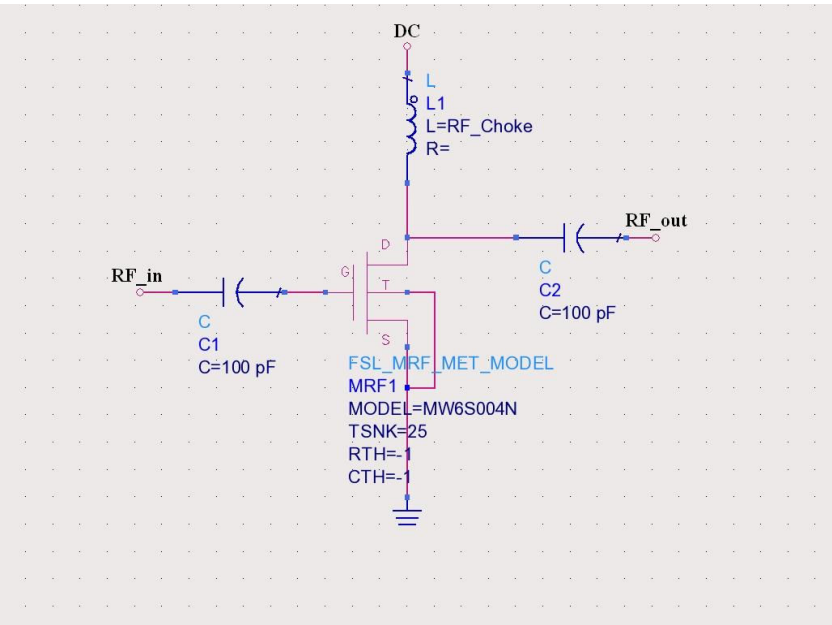

Figure 4.8: Basic DC Biasing Network

There are 3 criteria that must be considered in RF-choke design.

i. It must have enough impedance at low frequencies ($X_L = jwL$). Because, at 500MHz the impedance of the RF-choke decreases and it might tend to create loss for RF signal. So the RF-choke must have sufficient impedance at lower frequencies.

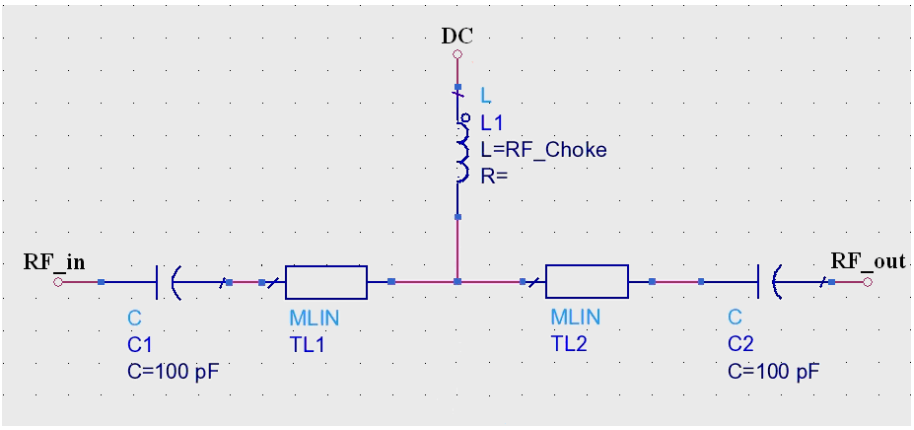

Figure 4.9: The position of RF-choke on RF transmission line

ii. There is no “perfect” components, and inductors are certainly no exception. The inductor is probably the components most prone to very drastic changes over frequency. Figure 4.10 shows what an inductor really looks like at radio frequencies.

Whenever two conductors are brought into close proximity but separated by a dielectric, and place a voltage differential between the two, a capacitor is formed. Thus, if any wire resistance at all exists, a voltage drop will occur between the windings, and small capacitors will be formed. This effect is shown in figure and is called distributed capacitance (C_d).

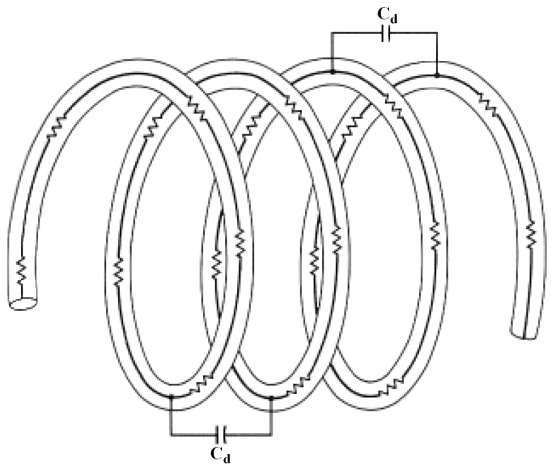

Figure 4.10: Distributed capacitance and series resistance in an inductor

Then, in Figure 4.11 below, the capacitance (C_d) is an aggregate of the individual parasitic distributed capacitances of the coil shown in Figure 4.10 [23].

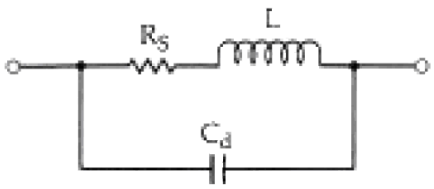

Figure 4.11: Inductor equivalent circuit

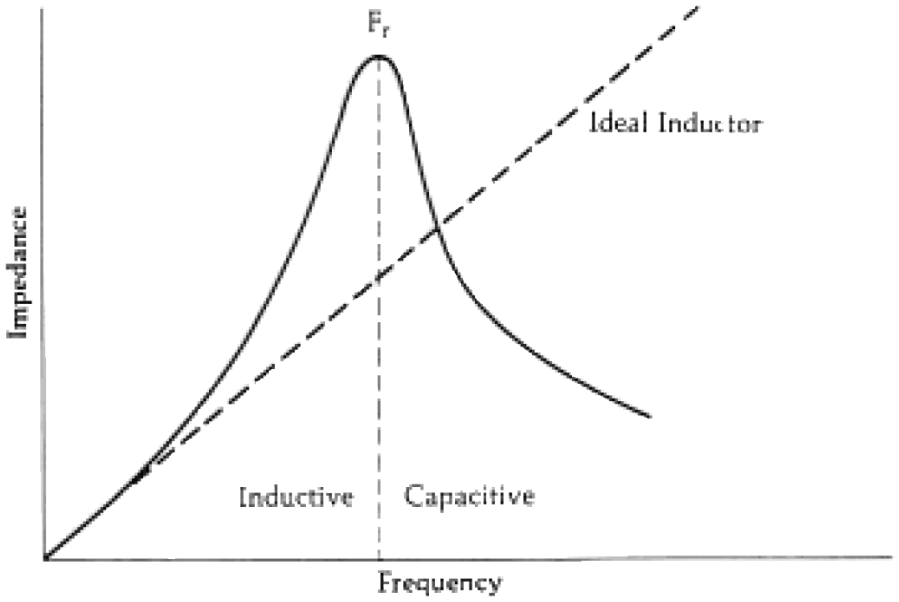

Figure 4.12: Impedance characteristic vs. frequency for a practical and an ideal inductor.

Resonance frequency, which is created by the inductor and layout effects, has to be put out of the whole band (500MHz-2GHz).

iii. Power amplifiers need sufficient DC current to handle the RF power specifications. This current passes through the RF-choke to reach the transistor, so thermal analysis is needed on the RF-choke. Consequently, DC current criteria must be taken into the consideration when a choke is designed.

Since the amplifier works in broadband, there is a trade off between the first and the second above criterias for designer. The first criteria can be obtained easily by using a high value inductive component. But in this situation, probably the resonance frequency of the inductor exists in the working frequency band. As a result, there is a need for making an optimization between these two criteria for avoiding the possible problems.

Various application notes are searched and then we decide to design the RF-choke not by only one inductor. The inductance value is shared to two inductors and they are connected in series. The inductance has been split up into two series connected elements to overcome the problems with parasitic capacitive coupling. Thus, a sufficiently high self-resonance frequency (SRF) has been obtained [22].

Coilcraft company's Mini/Midi Spring Air Core Inductors are chosen for RF-choke design. These inductors are chosen because of these reasons; the self-resonance frequencies of them are out of our working band, and I_{rms} values of them are enough for our application.

Firstly, the design process begins with simulations on ADS. ADS models of these inductors are obtained from Coilcraft Company. Then, different values of inductors are tried in combinations of two series inductors.

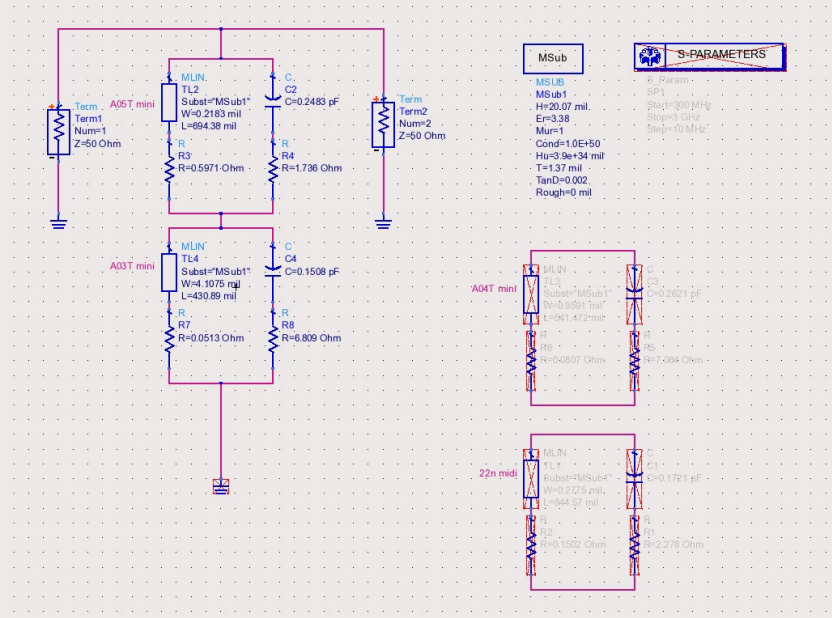

Figure 4.13: Simulation schematic of two series connected inductors for designing of RF-Choke

The below S-parameter graphs are obtained after the simulation of series connected Mini Spring Air Core Inductors A05T (18.5 nH) and A03T (8 nH). The above simulated circuitry is symmetric so there is no need to put S12 and S22 graph, because they are same as in order of S21 and S11 graphs.

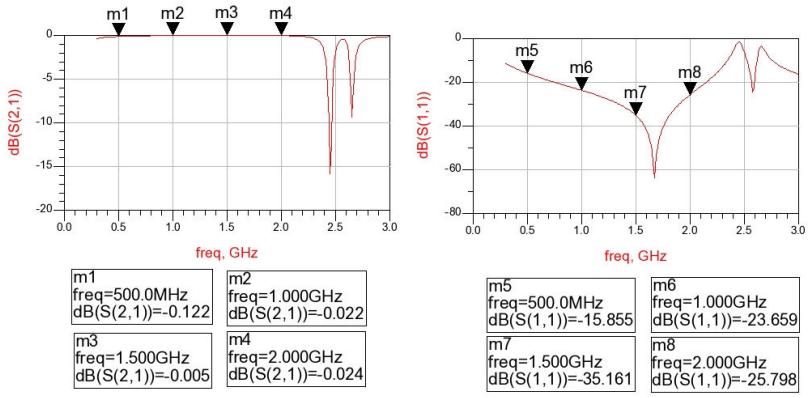

Figure 4.14: Simulation result of series connected Mini Spring Air Core Inductors A05T (18.5 nH) and A03T (8 nH)

As seen from the above figure, S21 is almost lossless, and S11 value is -15.8 dB at the worst case. As a comment, sufficient impedance value is achieved at low frequencies and resonance frequency of the inductors in combination is out of the working frequency band (@2.45 GHz). These simulated inductors are put on the board and these results are measured.

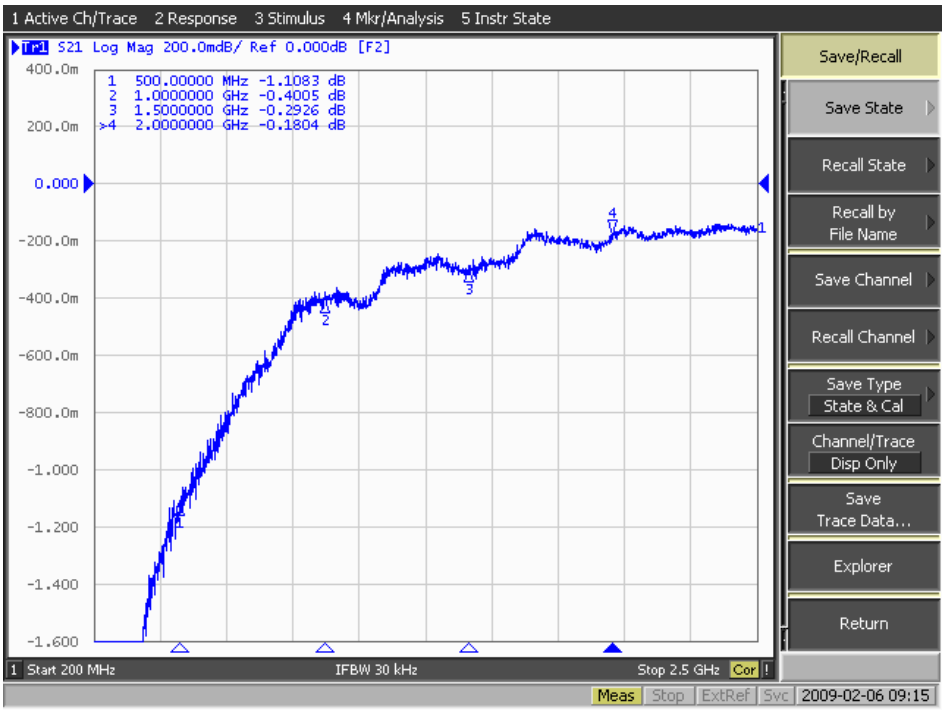

Figure 4.15: Measurement S21 result of series connected Mini Spring Air Core Inductors A05T (18.5 nH) and A03T (8 nH)

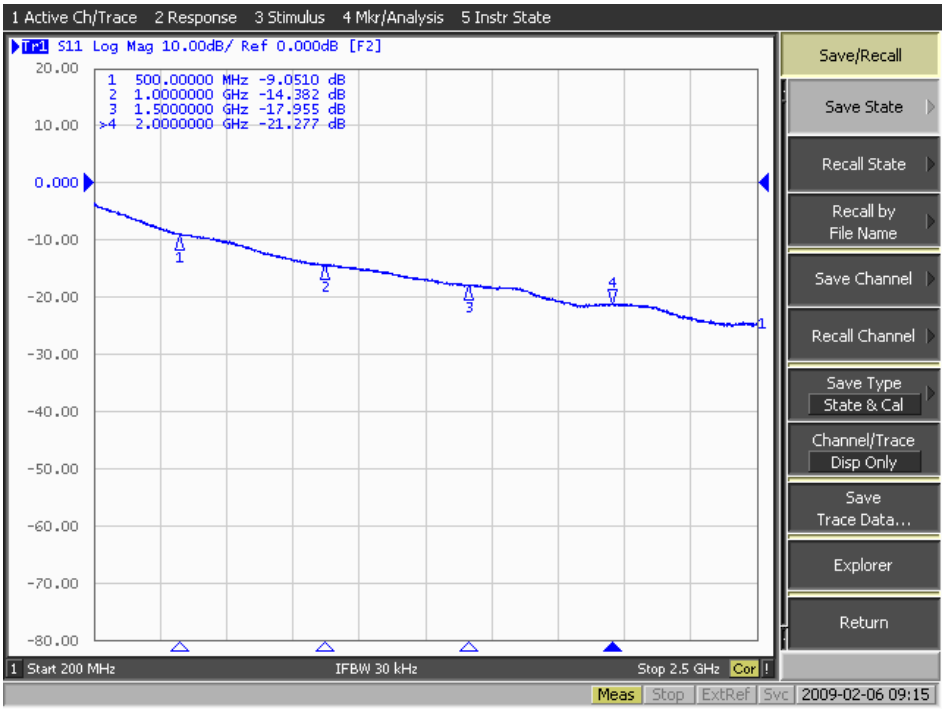

Figure 4.16: Measurement S11 result of series connected Mini Spring Air Core Inductors A05T (18.5 nH) and A03T (8 nH)

According to the above two graphs, it is understood that series connected A05T (18.5nH) and A03T (8nH) can not generate enough impedance at low frequencies. As seen from the S21 graph, 1.1 dB insertion loss is formed at 500MHz.

To get enough impedance at low frequencies, inductance value has to be increased. Coilcraft Midi Spring Air Core Inductors of 22nH and Mini Spring Air Core Inductors of A03T (8nH) are connected in series.

In first try, we see that resonance frequency of the RF-choke exists in the working frequency band. We think that parasitic effects can cause this problem. We determine that capacitive effect occurs between the ground area at the bottom side of the printed circuit board and the component pads that are at the upper side of the printed circuit board. To decrease the parasitic effect that occurs from the printed

circuit board, and to take the resonance frequency out of 500MHz-2000MHz band, the ground area at the bottom side of the RF-choke is removed.

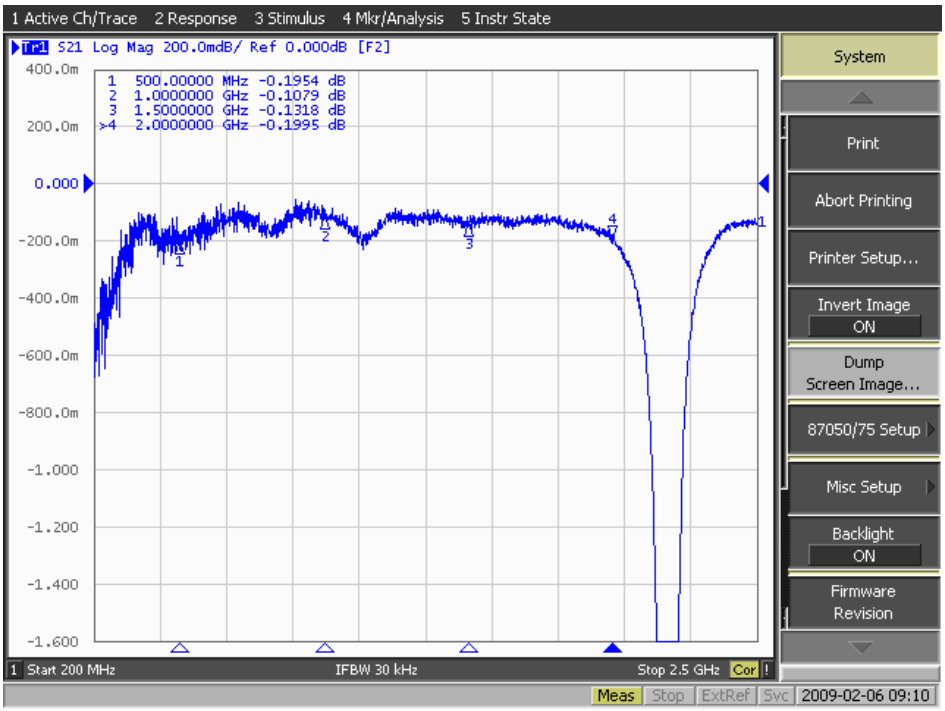

Figure 4.17: Measurement S21 result of series connected Midi Spring Air Core Inductors of 22nH and Mini Spring Air Core Inductors of A03T (8 nH)

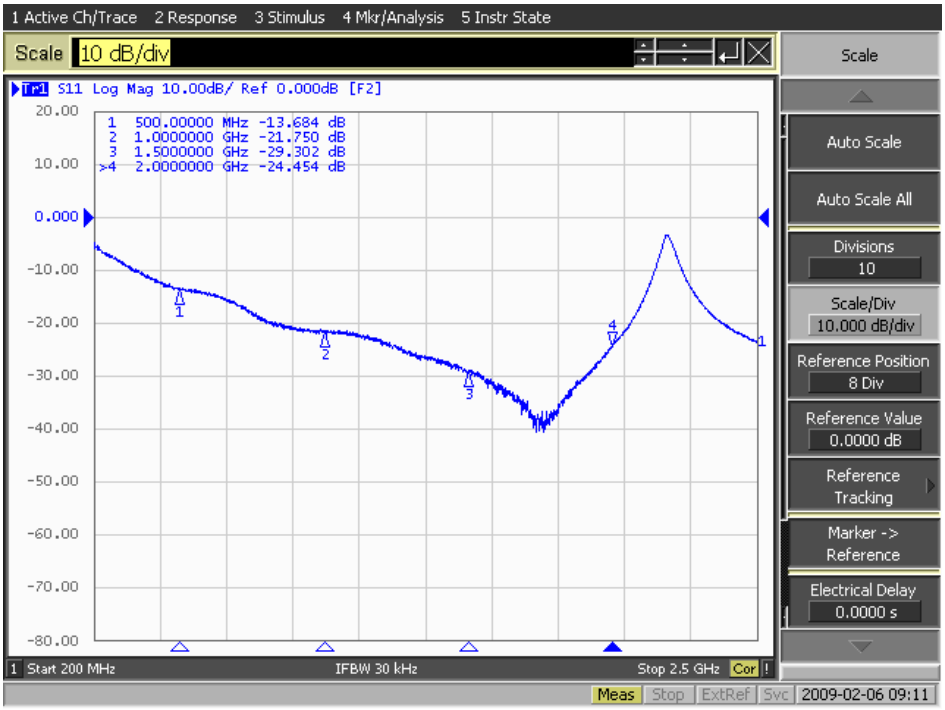

Figure 4.18: Measurement S11 result of series connected Midi Spring Air Core Inductors of 22nH and Mini Spring Air Core Inductors of A03T (8 nH)

As seen from the above graphs, although the resonance frequency comes closer (@2.2GHz) to the working frequency band, low insertion loss is obtained at the whole band; maximum S21 value is -0.2dB at 2GHz. In addition to this, sufficient return loss is obtained at the whole band too; minimum S11 value is -13.6dB at 500MHz.

4.3.3. SIMULATION METHODS

4.3.3.1. MODEL VERIFING

It's important to verify the ADS model of the driver stage MW6S004NT1 transistor to be able to sure of the truth of the model. The ADS model of the driver stage MW6S004NT1 transistor is verified in simulation, according to the s-parameter information in data sheet that is supported by Freescale Company. In verification process, no input and output matching networks, and no feedback components (for stability) is put in the circuitry, only the transistor and the biasing components are used and the transistor is directly connected to 50 ohm terminations.

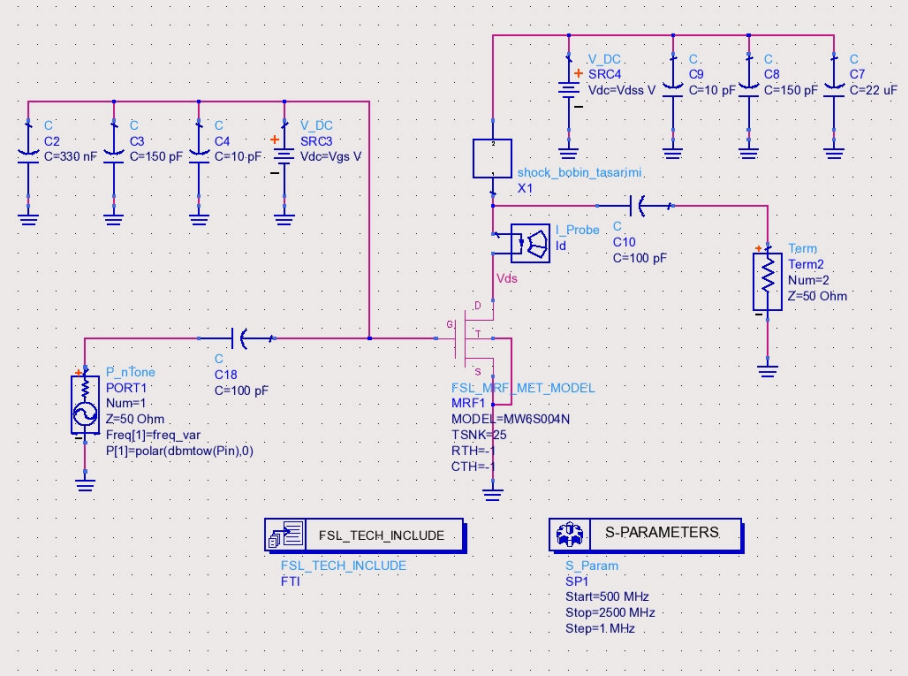

Figure 4.19: Simulation schematic for verifying the model of MW6S004NT1 transistor

The bias value of the transistor is adjusted according to the data sheet ($V_{dss} = 28V$, $I_{dq} = 50mA$), then the small signal s-parameters of the transistor are

simulated. The following graphs show the comparison of the s-parameter values which are taken from the data sheet, and the results of the simulation of the transistor model.

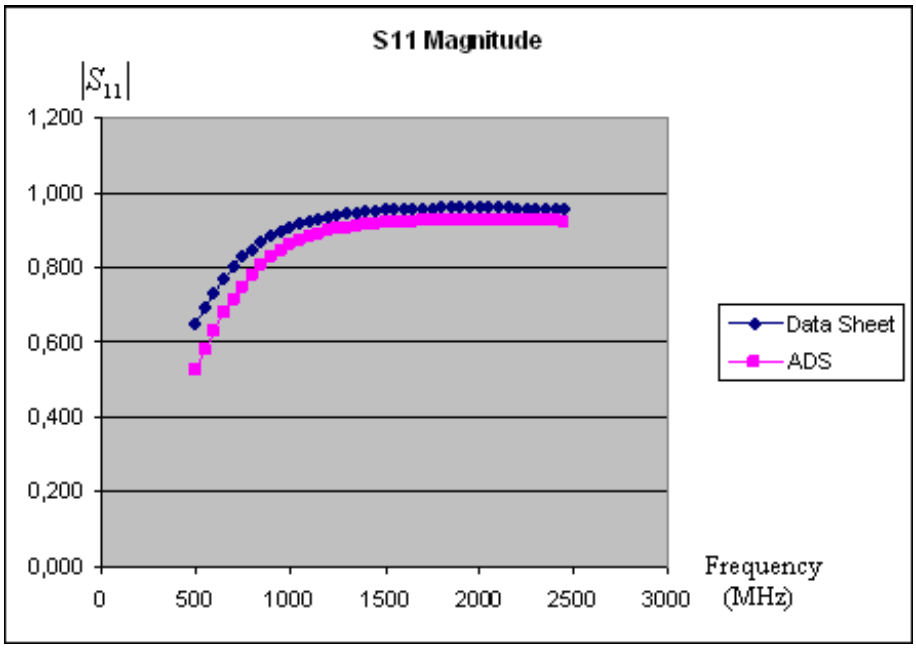

Figure 4.20: Comparison result of $|S_{11}|$ on verified MW6S004NT1 ADS model

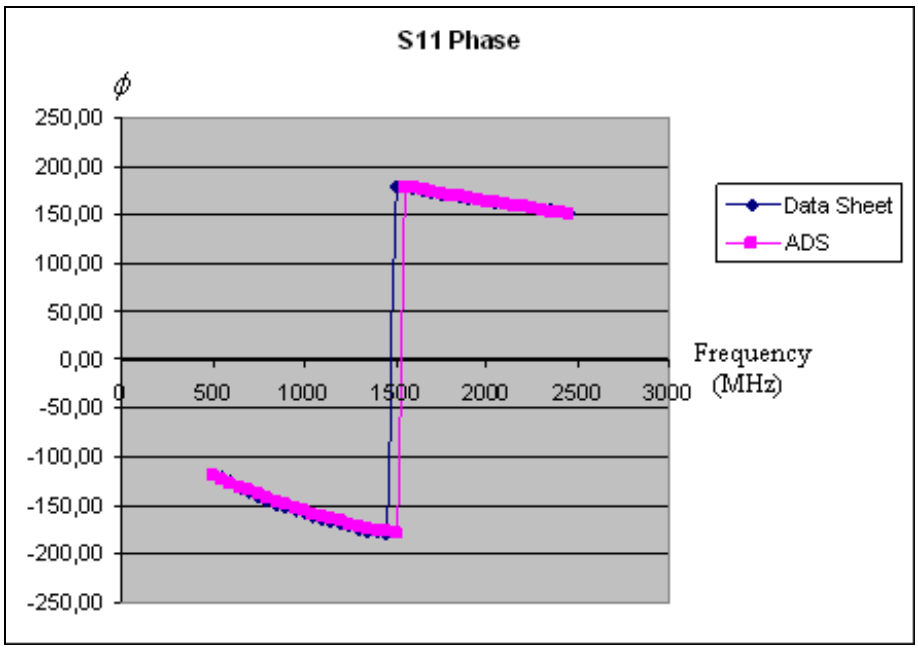

Figure 4.21: Comparison result of $\angle S_{11}$ on verified MW6S004NT1 ADS model

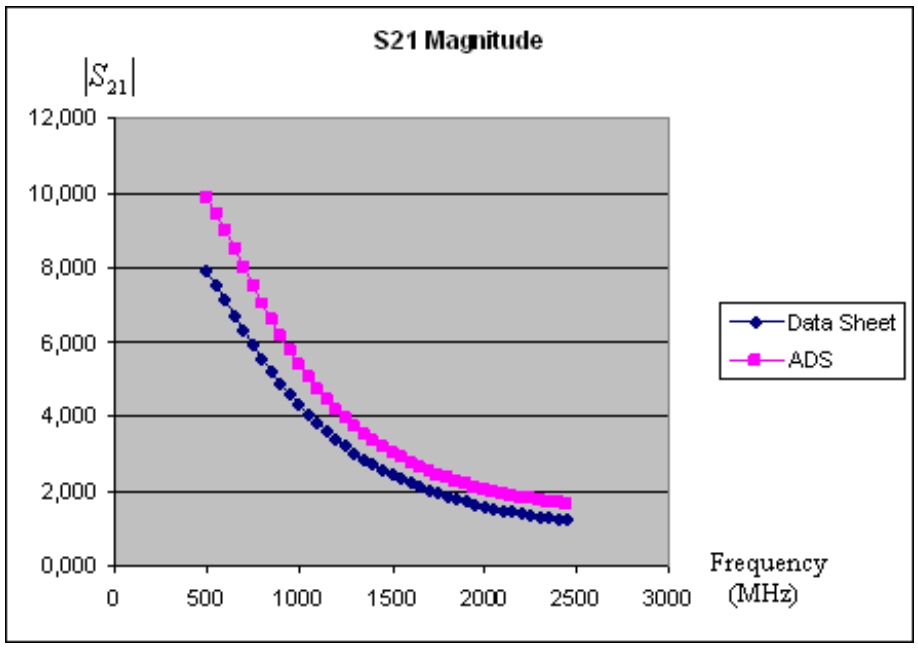

Figure 4.22: Comparison result of $|S_{21}|$ on verified MW6S004NT1 ADS model

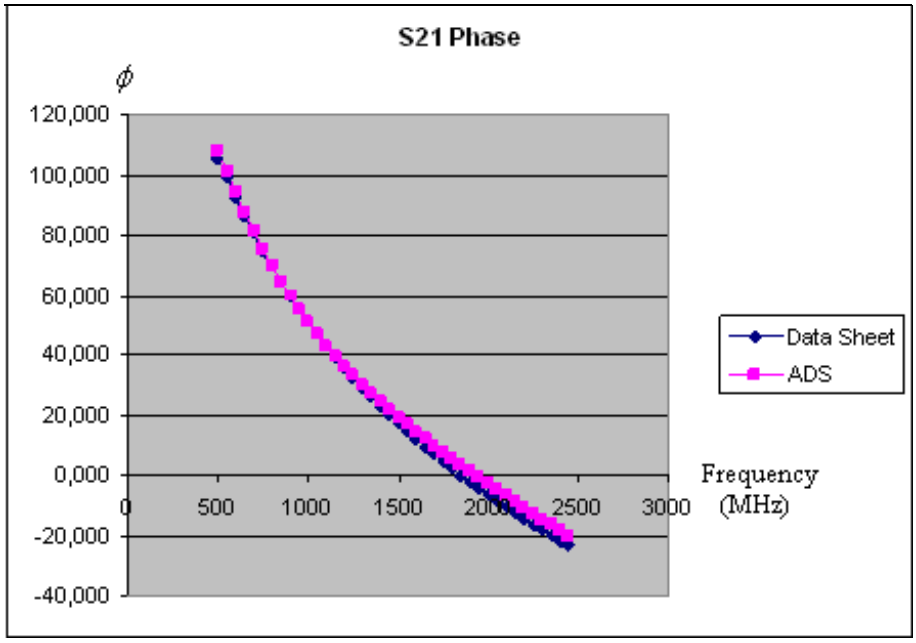

Figure 4.23: Comparison result of $\angle S_{21}$ on verified MW6S004NT1 ADS model

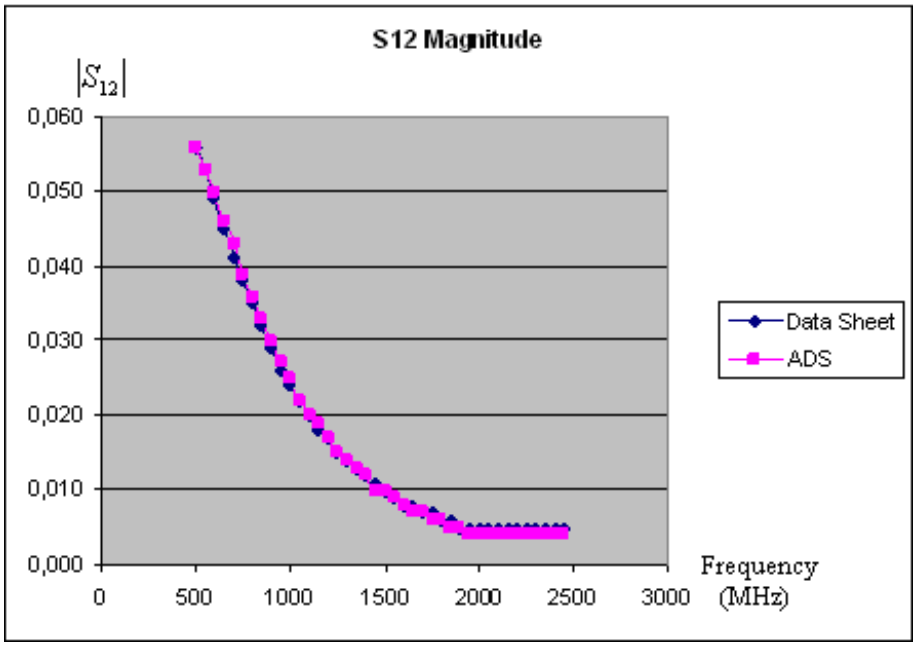

Figure 4.24: Comparison result of $|S_{12}|$ on verified MW6S004NT1 ADS model

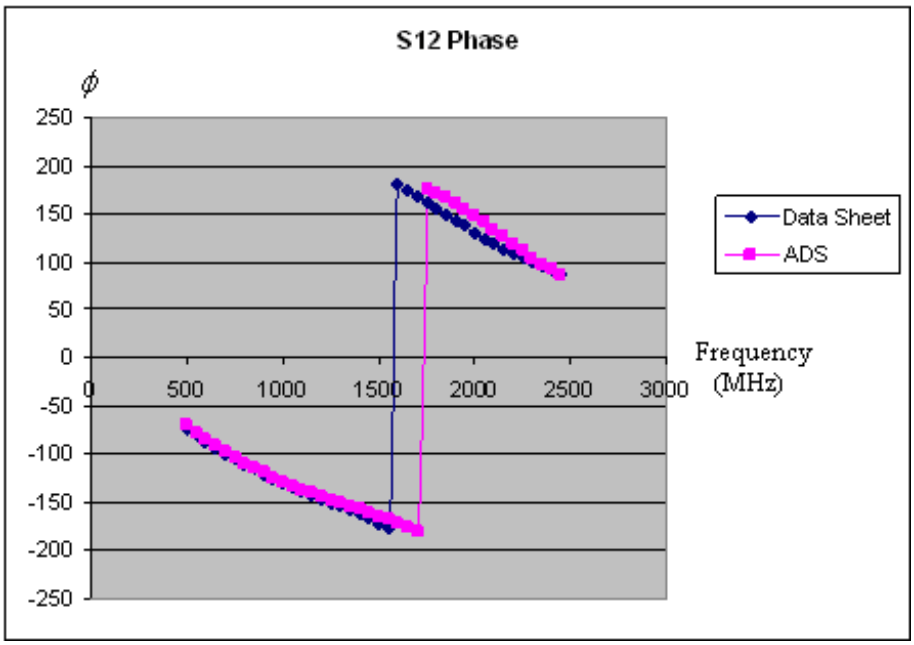

Figure 4.25: Comparison result of $\angle S_{12}$ on verified MW6S004NT1 ADS model

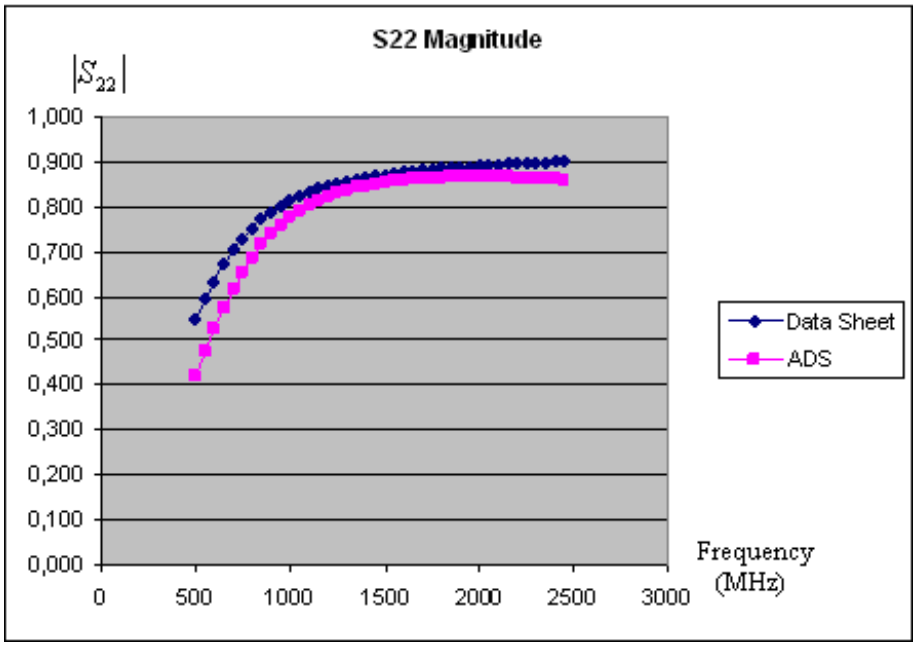

Figure 4.26: Comparison result of $|S_{22}|$ on verified MW6S004NT1 ADS model

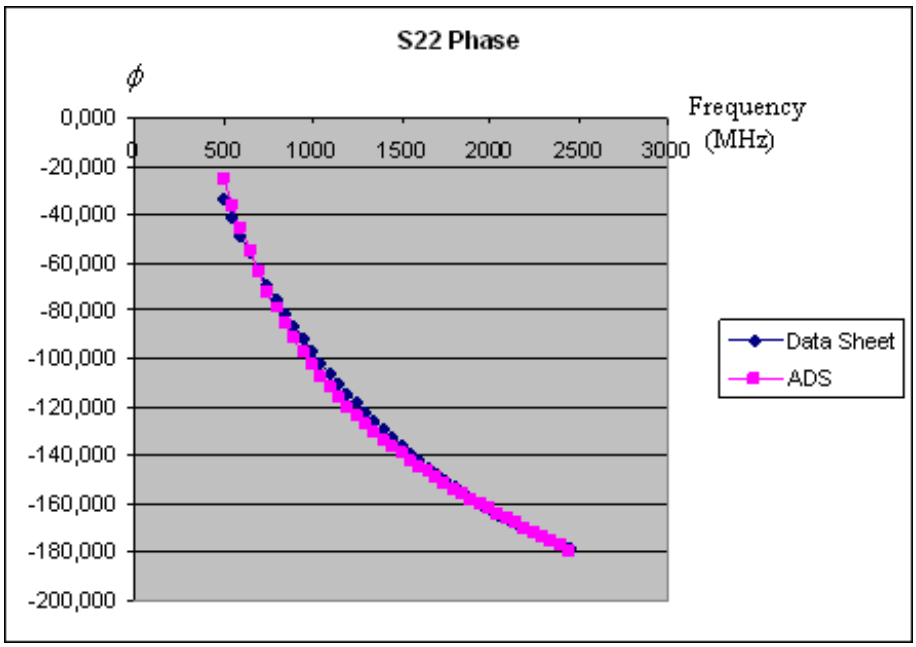

Figure 4.27: Comparison result of $\angle S_{22}$ on verified MW6S004NT1 ADS model

As seen from the above graphs, s-parameter values in the transistor's data sheet are very close to the values taken from simulation so, it can be said that ADS model of MW6S004NT1 transistor is well developed for simulation.

4.3.3.2. STABILTY

The unconditionally stable case occurs when $K > 1$ and $|\Delta| < 1$, and any passive source and load terminations can be used.

$$K = \left\{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11} \times S_{22} - S_{12} \times S_{21}|^2\right\} / \left\{2 \times |S_{12} \times S_{21}|\right\} \quad (4.1)$$

$$|\Delta| = |S_{11} \times S_{22} - S_{12} \times S_{21}|^2 \quad (4.2)$$

$$B = 1 + |S_{11}|^2 - |S_{22}|^2 - |S_{11} \times S_{22} - S_{12} \times S_{21}|^2 \quad (4.3)$$

The condition $K > 1$ is only a necessary condition for unconditional stability. Therefore, a simultaneous conjugate match having unconditional stability is possible if $K > 1$ and $|\Delta| < 1$ ($|\Delta| < 1$ implies that $B > 0$) [24].

Setup measurements are done simultaneously with simulations on ADS. Feedbacks are taken from the setup measurements, and then the lumped components and the parasitic effects of them are tried to be modeled in simulation.

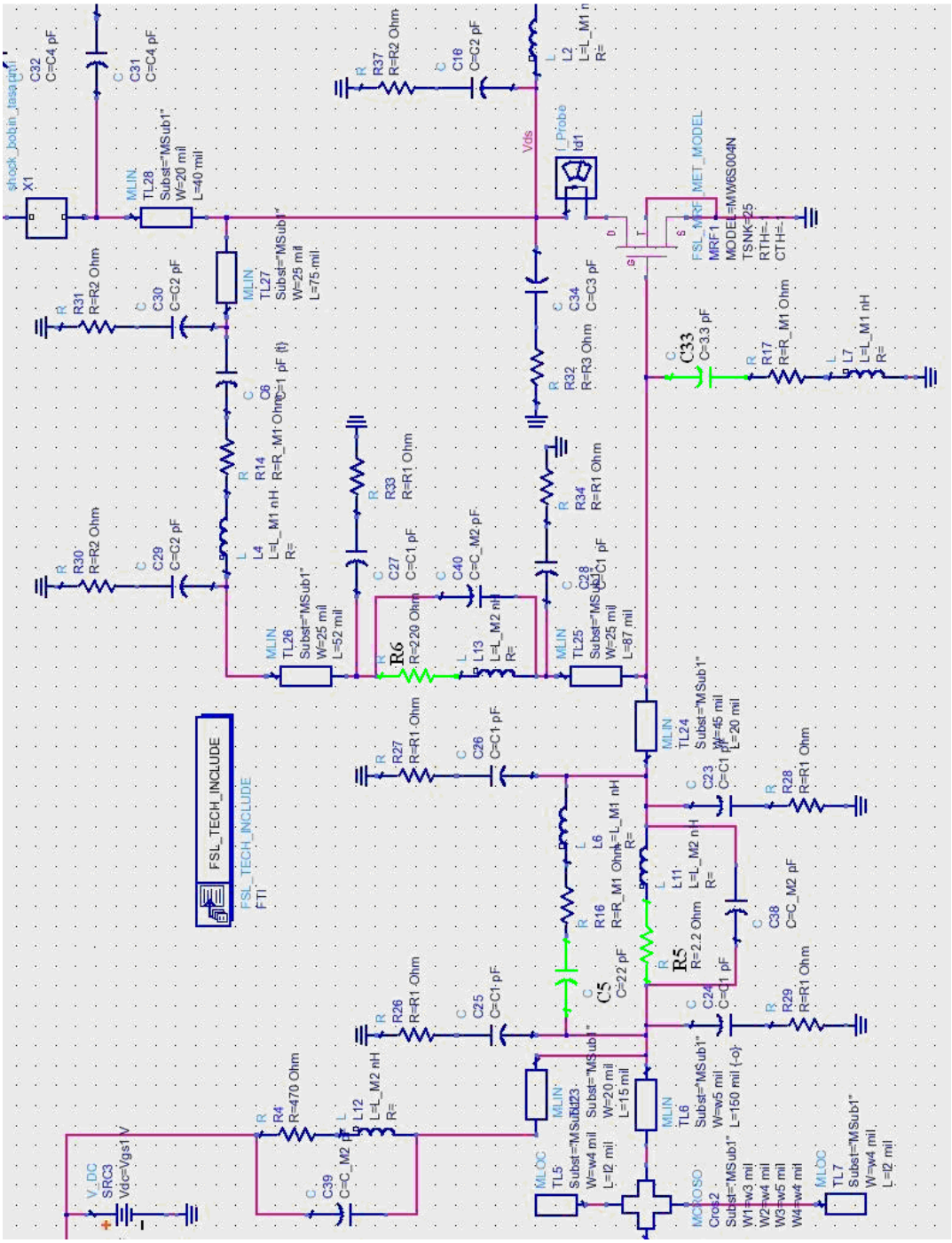

Figure 4.28: Stability analysis that show the optimized components to obtain unconditionally stable case for driver stage configuration

By using the feedback resistor (R6), the series gate resistor (R5), and the parallel capacitor (C5) over the series gate resistor which optimize the gain at high frequencies, in addition, the capacitor (C33) between the gate and the ground that improves the matching and S21; are modeled in simulation. Stability Factor (K) and Stability Measure (B) values are observed in ADS.

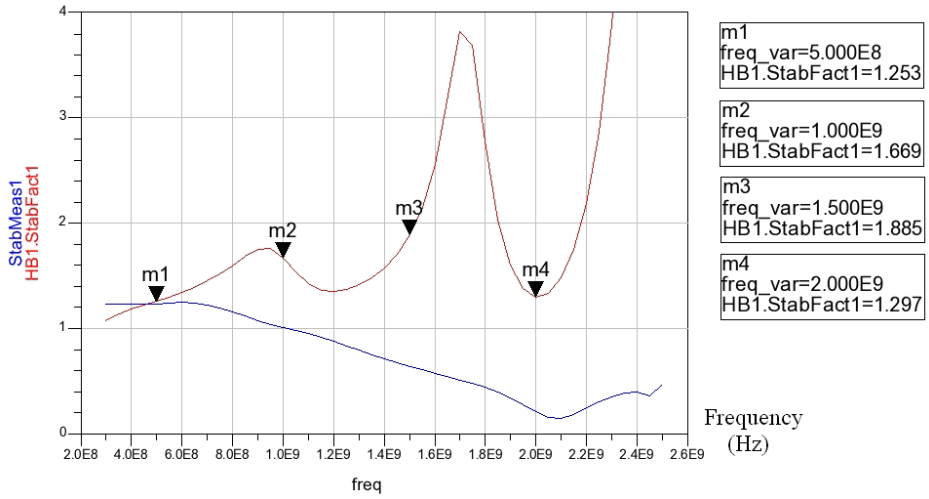

Figure 4.29: Graph of Stability Factor (K) and Stability Measure (B) for driver stage

As seen from the above graph, the circuitry behaves as stable (Stability Factor>1 and Stability Measure>0).

4.3.3.3. SCATTERING PARAMETERS

We have aimed 37dBm (5W) output power taken from two stage power amplifier configuration so; the output of the driver stage have to be approximately 27dBm. At the whole band, when we adjust the input power to obtain 27dBm power at the driver stage output, we can find the large signal scattering parameters of this stage.

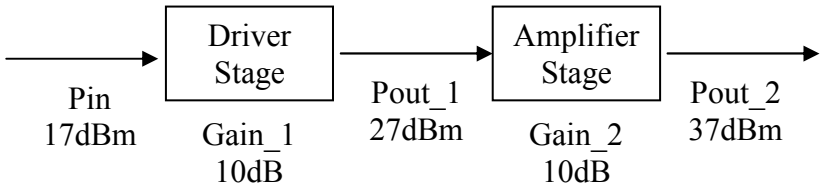

Figure 4.30: Complete topology in general

The input and the output matching networks are optimized in simulation by tuning the length and width of the microstrip lines and open circuit stubs. This simulation is done by using Harmonic Balance Simulation of LSSP (Large Signal S-Parameter) tool in ADS when 5W output power is obtained at the output of the overall system. When we look MW6S004NT1 transistor in single stage configuration, these large signal s-parameters graphs are obtained in simulation.

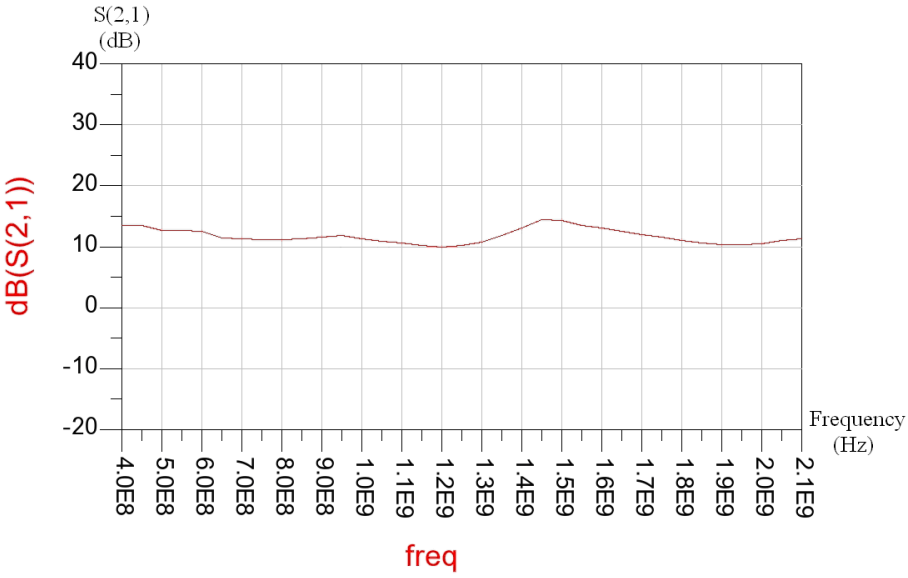

Figure 4.31: The simulation result of LSSP of S_{21} for driver stage configuration

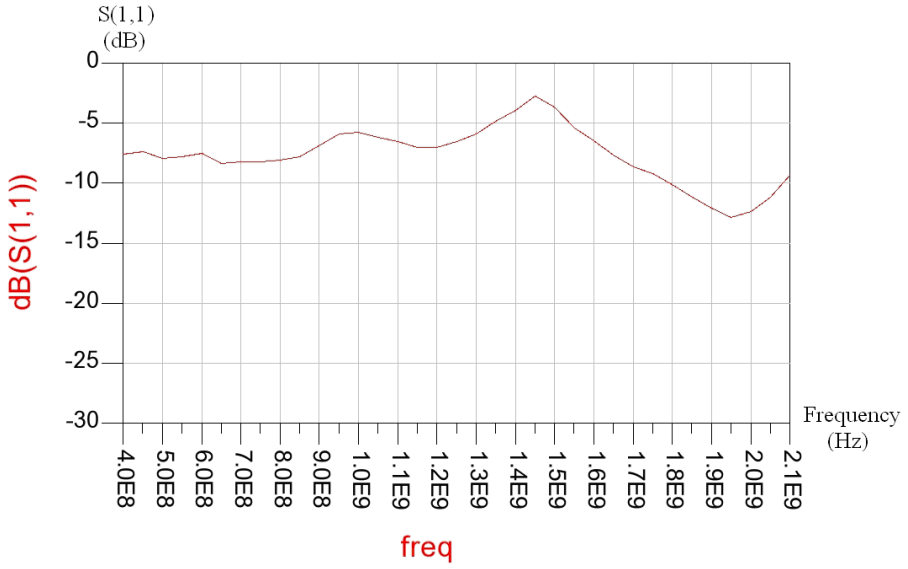

Figure 4.32: The simulation result of LSSP of S_{11} for driver stage configuration

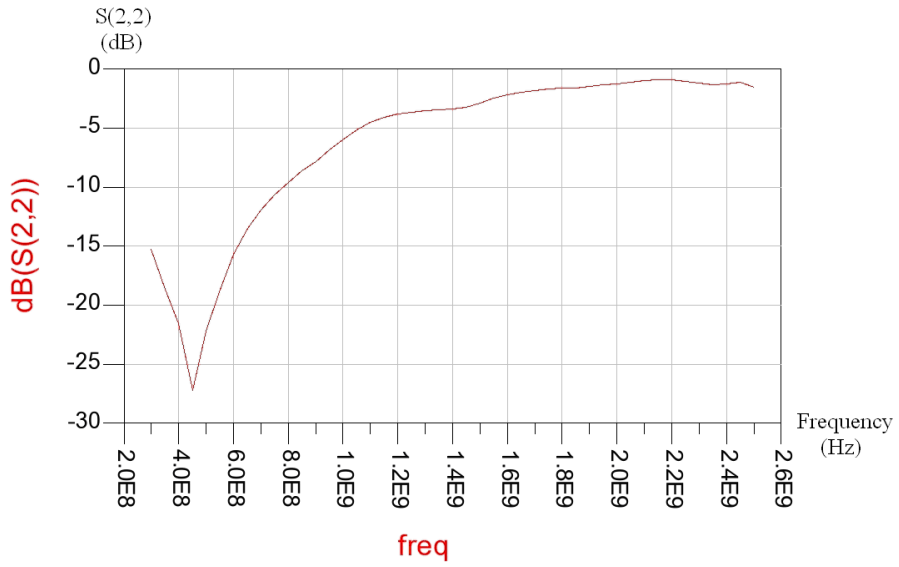

Figure 4.33: The simulation result of LSSP of S_{22} for driver stage configuration

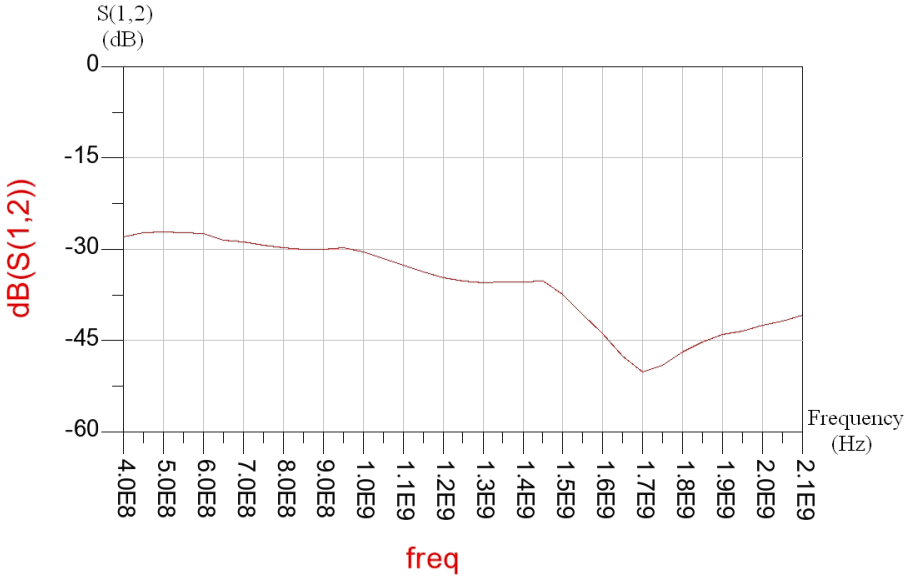

Figure 4.34: The simulation result of LSSP of S_{12} for driver stage configuration

4.3.3.4. INTERMODULATION DISTORTION

The simulation of IMD is done with two equal power input signals and there is 1 MHz difference between them. In simulation, the output power of the single stage configuration is arranged to 27dBm. Two equal power signals are given to the system, so Peak Envelope Power (PEP) of these two signals has to be 27dBm. The PEP is assumed to be twice the RMS power indicated, ignoring the harmonic content of the output signal [25]. If the voltage level of single tone is assumed to be V then the voltage level of each one of these two tones have to be $V/2$. As known, power is related to square of voltage. As a result, power levels of these to signal have to be 4 times (6dB) lower than power level of single tone. Following figures show IMD results at different frequencies.

$fc1 = 500MHz, fc2 = 501MHz$:

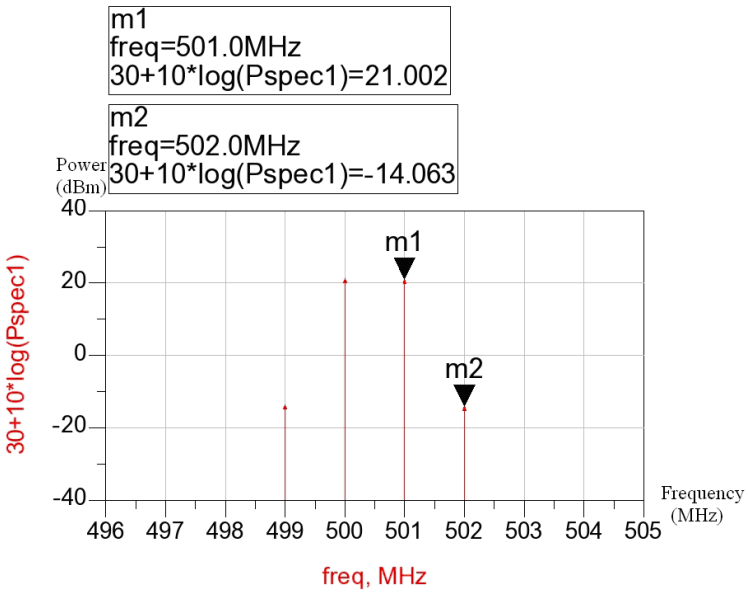

Figure 4.35: The simulation result of IMD at 500MHz for driver stage configuration

$fc1 = 1000MHz, fc2 = 1001MHz$:

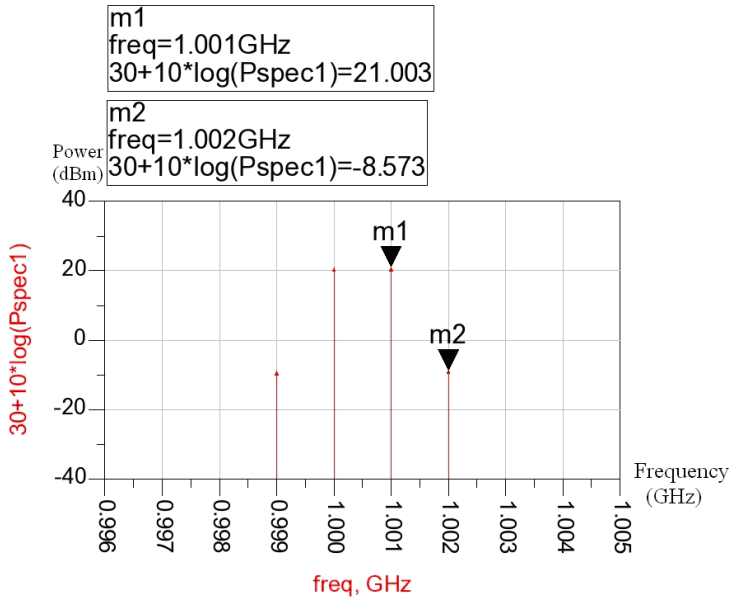

Figure 4.36: The simulation result of IMD at 1000MHz for driver stage configuration

$fc1 = 1500MHz, fc2 = 1501MHz$:

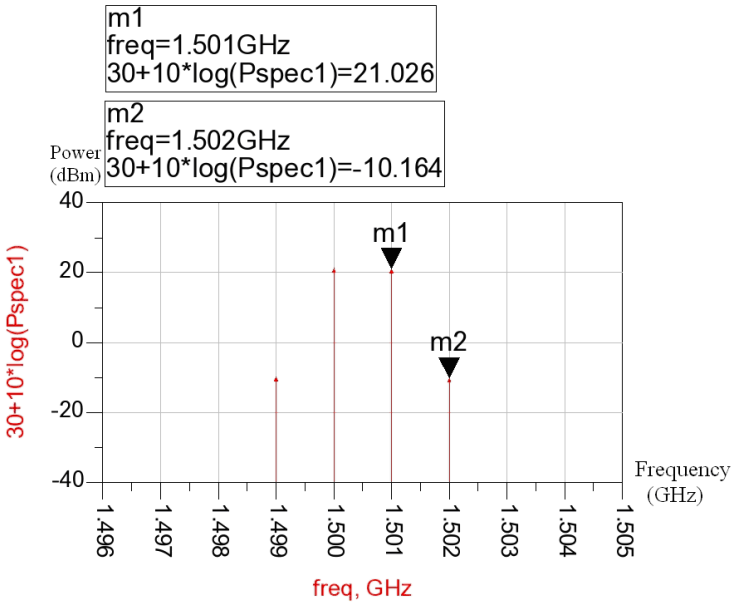

Figure 4.37: The simulation result of IMD at 1500MHz for driver stage configuration

$fc1 = 2000MHz, fc2 = 2001MHz$:

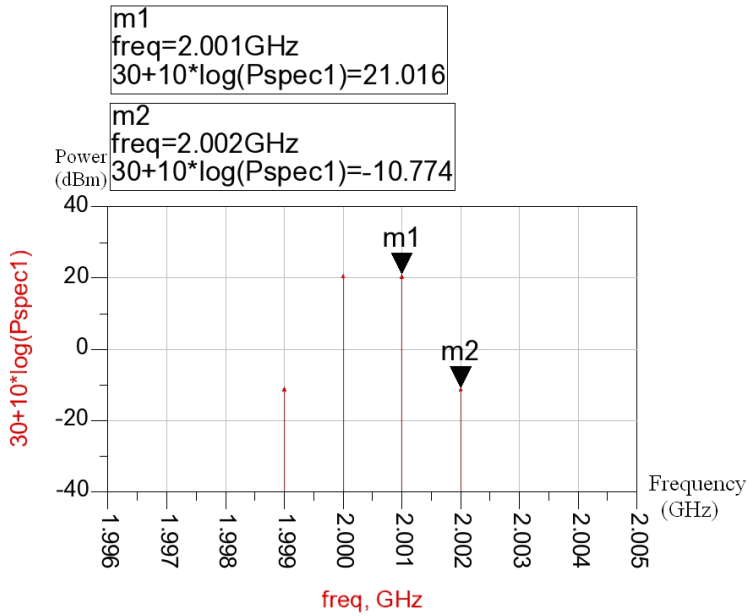

Figure 4.38: The simulation result of IMD at 2000MHz for driver stage configuration

As seen from the above graphs, the IMD value of the single stage system is simulated as -29.5dBc at worst case.

4.3.3.5. EFFICIENCY

The below graph shows efficiency values of the single stage configuration that are founded from the simulation.

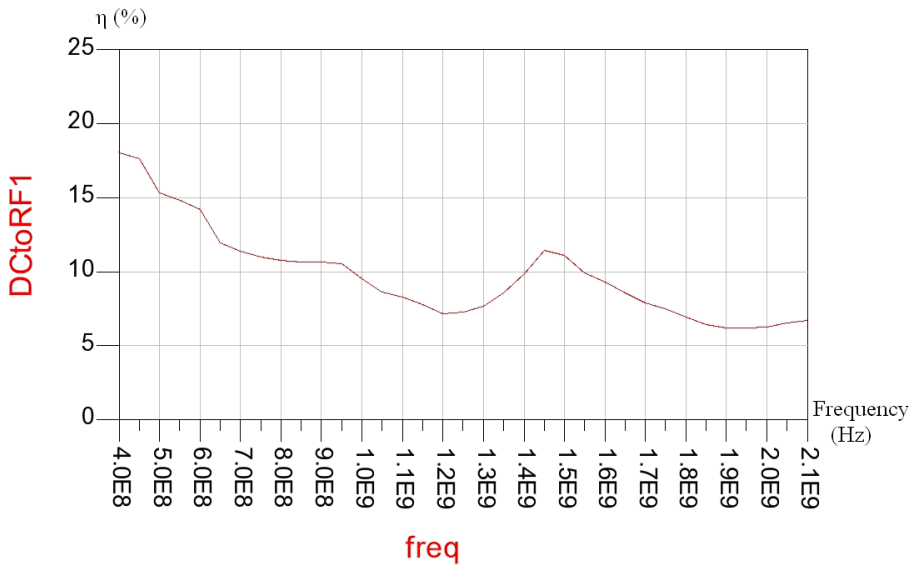

Figure 4.39: The simulation result of efficiency for driver stage configuration

The reason of getting the efficiency values worse above 1 GHz, (as said before) there isn't any inter circuit matching network between the two stages, so when the driver stage is analyzed separately, the output of the driver stage have to be terminated to 50 ohm. The output impedance of the driver transistor deviates from 50 ohm when frequency increases (see Figure 5.18). Because of this, the single stage amplifier configuration is forced to produce demanded output power at high frequencies.

4.3.3.6. 1dB COMPRESSION POINT

In simulation of the single stage configuration, the aim is getting 27dBm output power. The following graph shows the compression point of the single stage amplifier configuration, and it can be seen that the operation point where the transistor is in linear region or not, when it produces 27dBm output power.

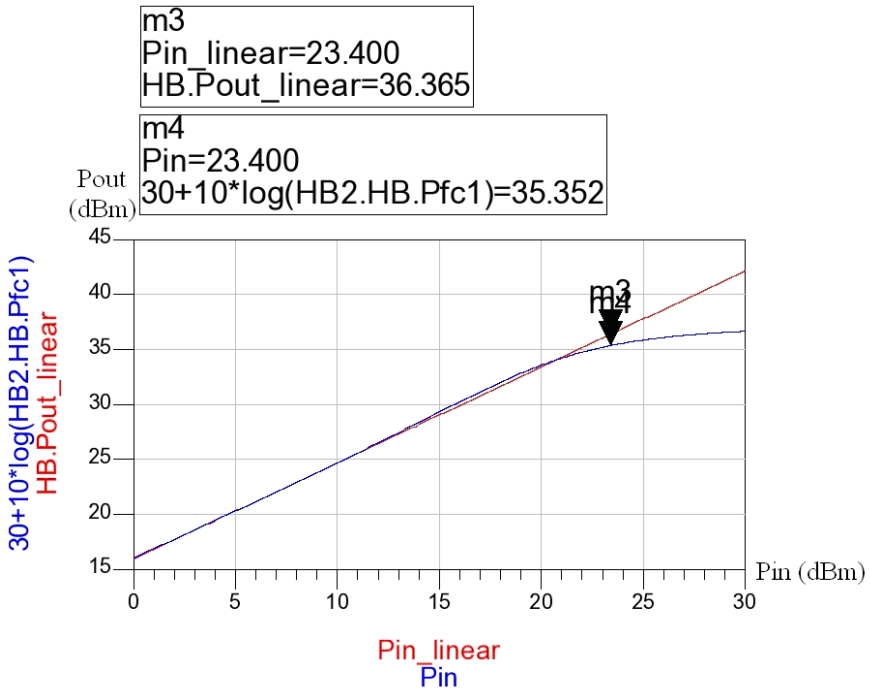

Figure 4.40: The simulation result of 1dB Compression Point for driver stage configuration

1dB compression point of the single stage amplifier configuration is approximately 35.3dBm. Whether it looks early to enter in compression region, the poorness of S22 values at frequencies above 1.5 GHz may cause this.

4.3.4. MEASUREMENT METHODS

4.3.4.1. STABILITY

The driver stage amplifier behaves as stable by using the feedback components which are found in simulation. There isn't any oscillation occurred during the measurement process.

4.3.4.2. SCATTERING PARAMETERS

Firstly, the single stage configuration is simulated, and the components that are found from simulation, is put onto printed circuit board. In first try, the simulation and measurement results don't match to each other. In other words, the results of simulation are better than measurement's. As said before, setup measurements are done simultaneously with simulations on ADS, and feedbacks are taken from the setup measurements. Then, according to the large signal s-parameter results taken from the setup measurements, the model of lumped components and the parasitic effects are optimized in simulation correctly.

By the way, generally parasitic effects can occur from the printed circuit board layout, coupling between the components or transmission lines, etc… The effect of parasitic increases when operating frequency increases.

As mentioned in "Designing of Choke" section, to decrease the parasitic effects of the power amplifier circuitry, the ground areas that are at the bottom side of the chokes and around the chokes, are removed. This causes to put the resonance frequency out of the operating frequency band. Furthermore, the ground area at the bottom side of the Drain pad of the transistor was removed. However this action improves the gain of the power amplifier, removing the ground area at the bottom

side of the Gate pad made the gain of the power amplifier worse, so the ground areas are removed only at the bottom side of the Drain pad and chokes. In addition, as mentioned in “Stability” section, putting a shunt capacitor between the gate of the transistor and the ground improves the gain of the amplifier. We think that, somehow, this capacitor improves the transistor matching. In a conclusion, to improve the gain and the matching of the power amplifier at broadband, transistor gate wants shunt capacitive impedance but drain doesn’t.

The graphs are given below that show the large signal s-parameter results of the measurement.

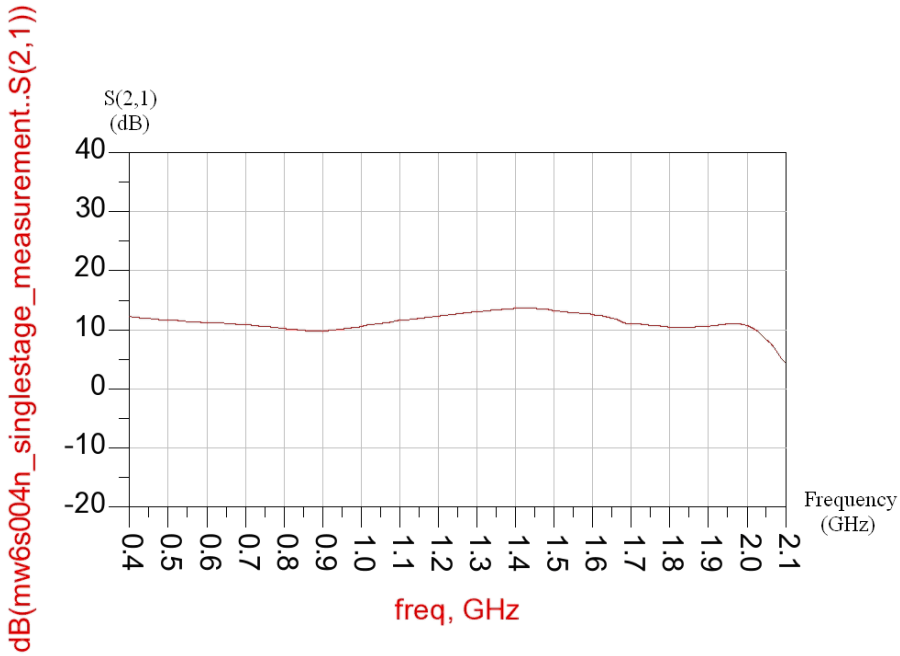

Figure 4.41: The measurement result of LSSP of S_{21} for driver stage configuration

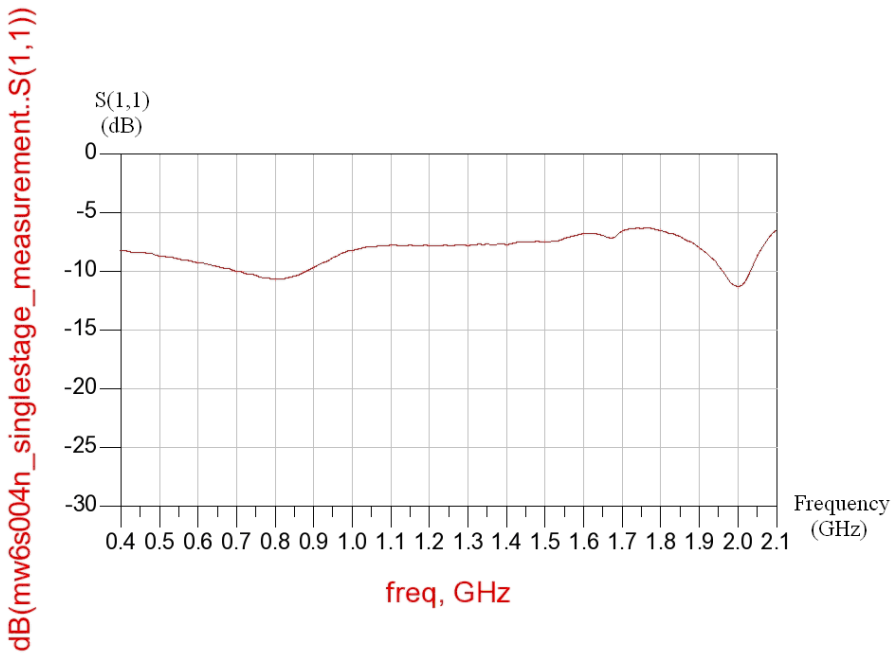

Figure 4.42: The measurement result of LSSP of S_{11} for driver stage configuration

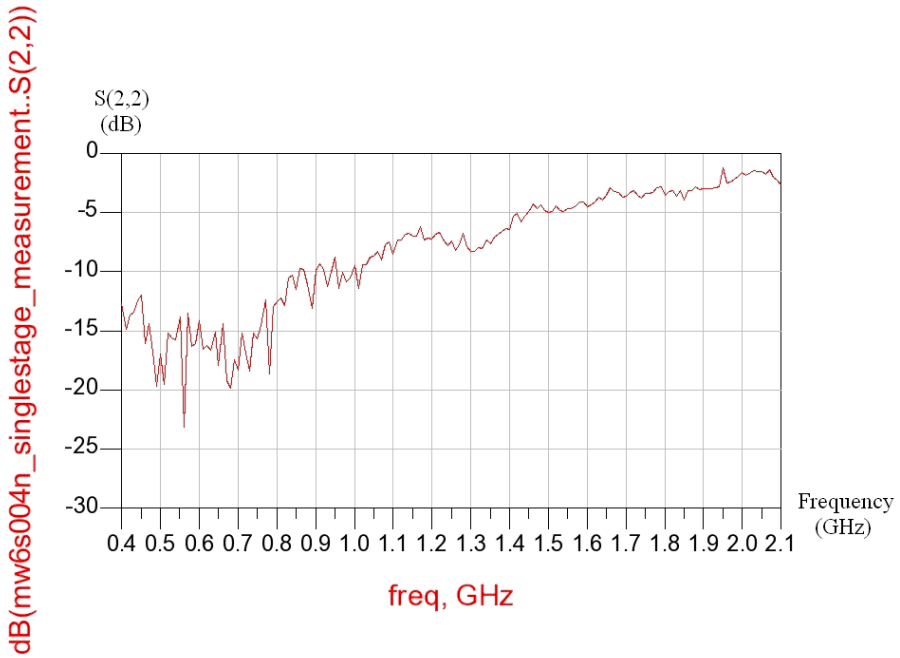

Figure 4.43: The measurement result of LSSP of S_{22} for driver stage configuration

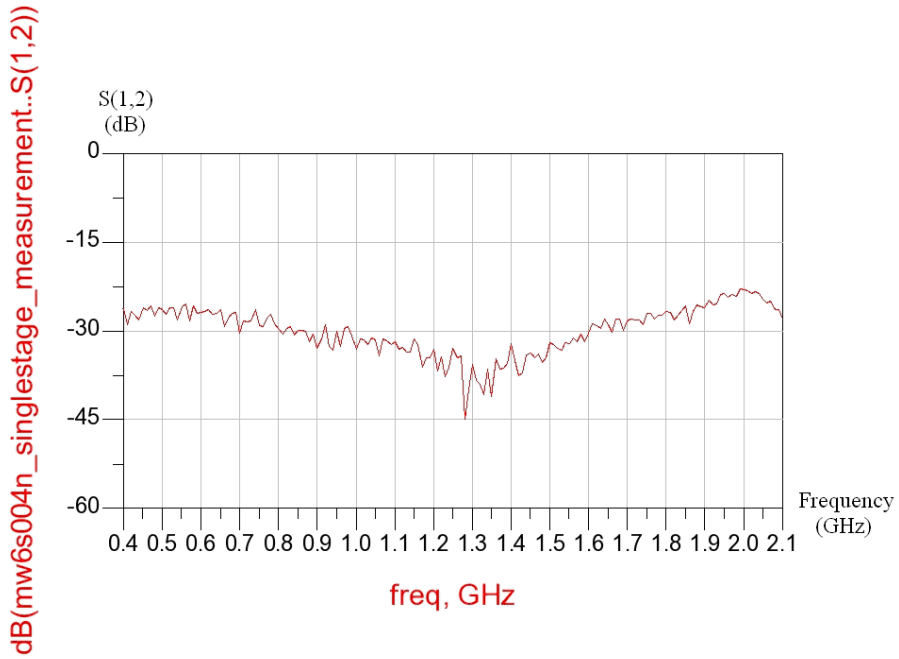

Figure 4.44: The measurement result of LSSP of S_{12} for driver stage configuration

4.3.4.3. INTERMODULATION DISTORTION

The setup below is established to measure IMD of the single stage configuration.

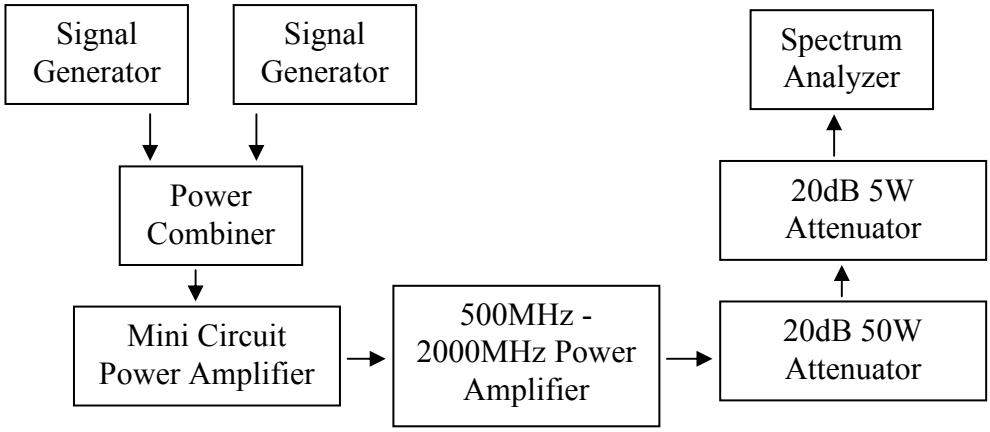

Figure 4.45: Setup is established to measure IMD
of single stage configuration

Two equal power input signals are generated by two signal generators, and they are summed in Power Combiner, then Mini Circuit Power Amplifier amplifies the summed signal to demanded input level of 500MHz-2000MHz Power Amplifier. This amplifier amplifies the summed input signal to 27dBm Peak Envelope Power, and then two attenuators attenuate this summed signal, finally, IMD can be measured in the Spectrum Analyzer.

The IMD of Mini Circuit Power Amplifier is measured as -50dBc. So, it can be said that this amplifier doesn't influence the IMD result of 500MHz-2000MHz Power Amplifier, because its IMD value is too low.

The results of IMD are given below for frequencies at 500MHz, 1000MHz, 1500MHz, and 2000MHz at 27 dBm Peak Envelope Power.

$fc1 = 500MHz, fc2 = 501MHz$:

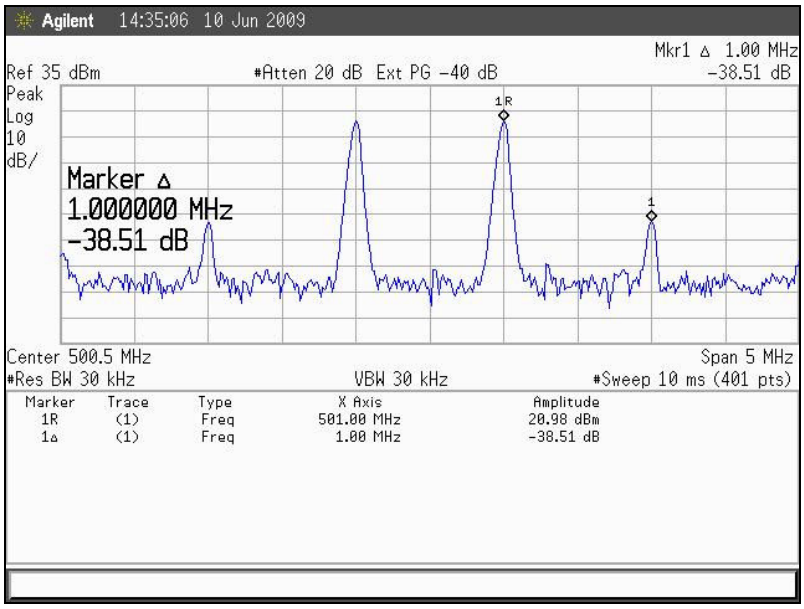

Figure 4.46: The measurement result of IMD at 500MHz for driver stage configuration

$fc1 = 1000MHz, fc2 = 1001MHz$:

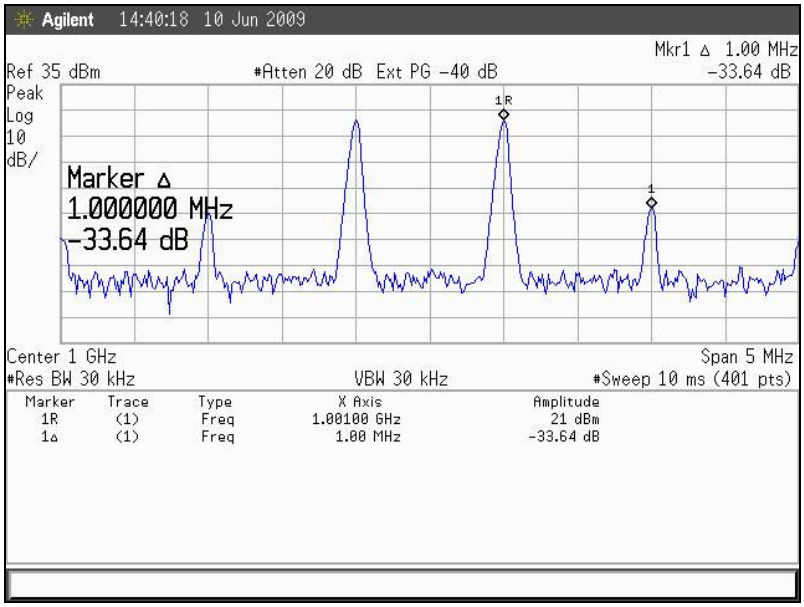

Figure 4.47: The measurement result of IMD at 1000MHz for driver stage configuration

$fc1 = 1500MHz, fc2 = 1501MHz$:

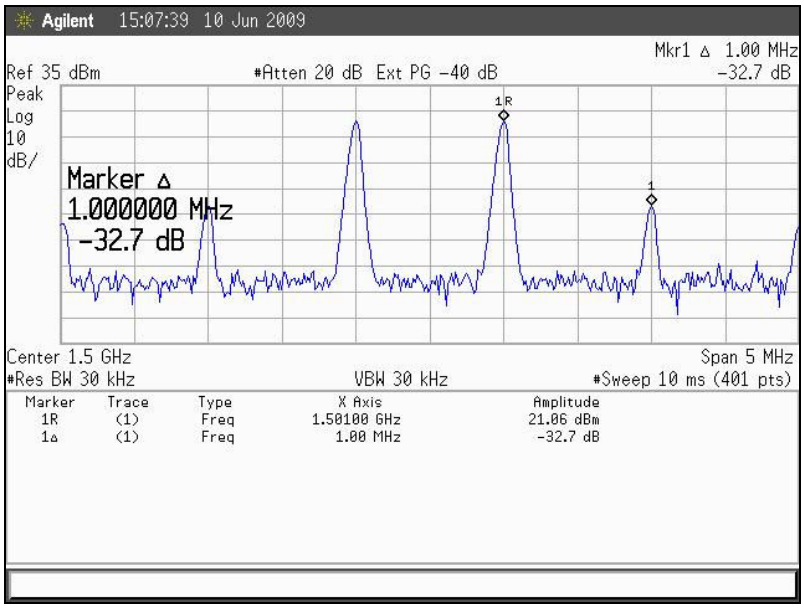

Figure 4.48: The measurement result of IMD at 1500MHz for driver stage configuration

$fc1 = 2000MHz, fc2 = 2001MHz$:

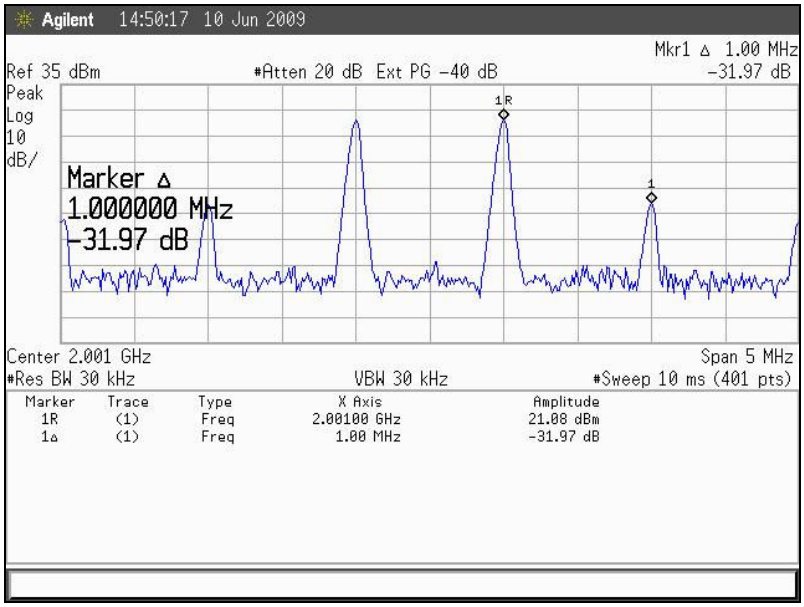

Figure 4.49: The measurement result of IMD at 2000MHz for driver stage configuration

As seen from the above graphs, the IMD result at 27dBm PEP over the whole band is better than -32dBc.

4.3.4.4. EFFICIENCY

In this section, the aim is not taking high power from driver stage so; there is no need to measure the efficiency of the transistor, because low input power is given to the driver stage. Thus, the transistor doesn't use considerable DC power to drive the input signal to last stage.

4.3.4.5. 1dB COMPRESSION POINT

In this section, there is no need to measure the 1dB compression point of the transistor, because low input power is given to the driver stage, this means, the aim is not taking high power from this stage.

4.3.5. COMPARISON BETWEEN SIMULATION & MEASUREMENT RESULTS

4.3.5.1. STABILITY

To obtain the stability of the transistor, the component values which are found from the simulation are suitable for measurements too. During the measurement process, there is no oscillation is seen at the whole band.

4.3.5.2. SCATTERING PARAMETERS

The graphs are given below that compare the large signal s-parameter results between the simulation and the measurement.

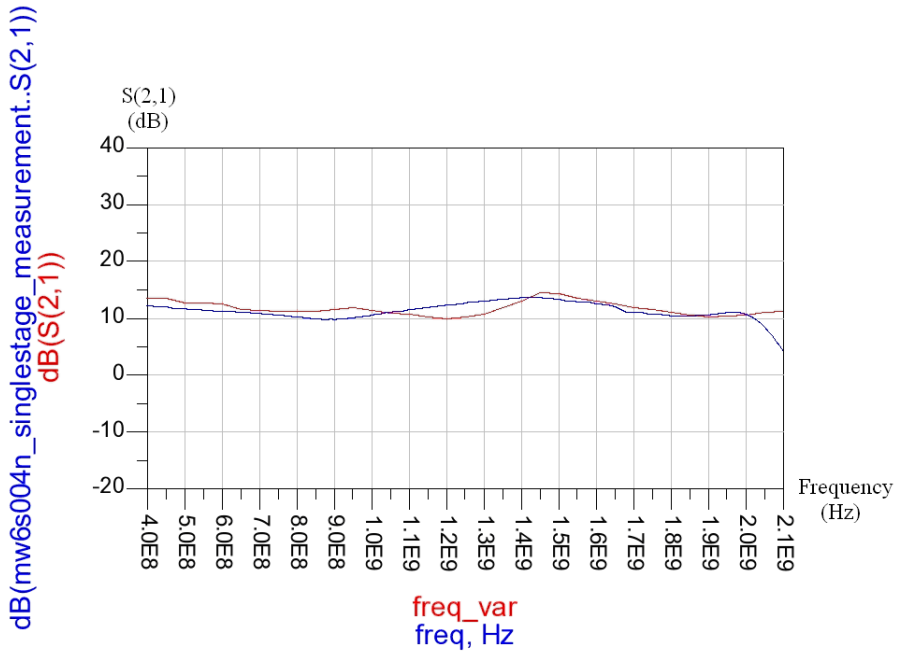

Figure 4.50: Comparison of LSSP result of S_{21} between simulation and measurement for driver stage configuration

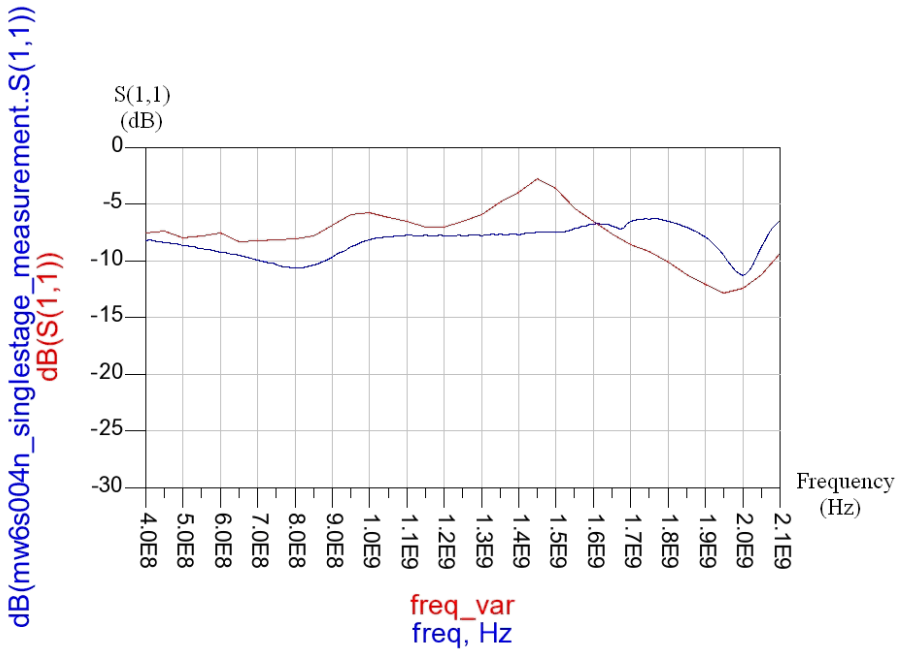

Figure 4.51: Comparison of LSSP result of S_{11} between simulation and measurement for driver stage configuration

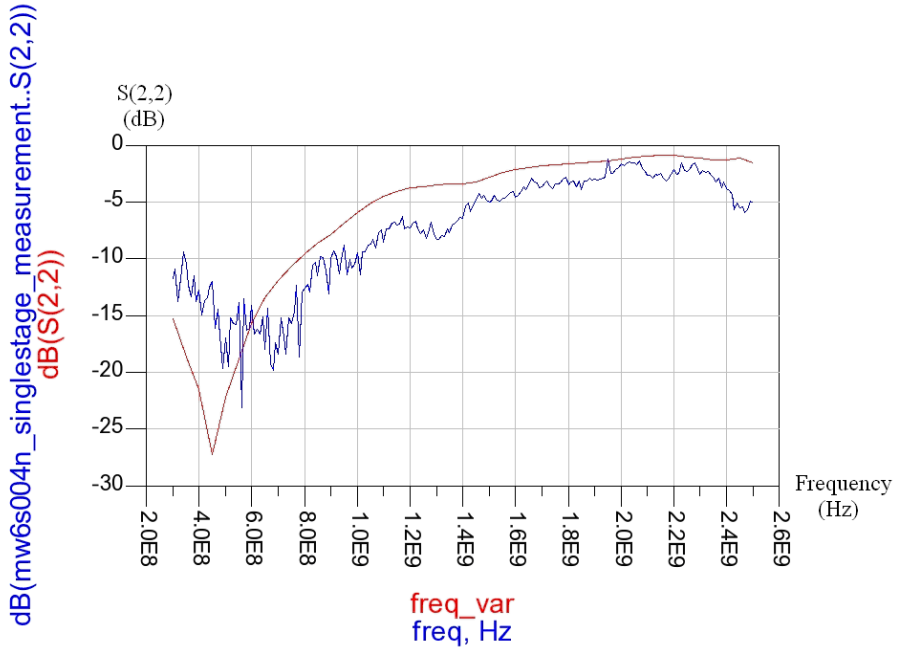

Figure 4.52: Comparison of LSSP result of S_{22} between simulation and measurement for driver stage configuration

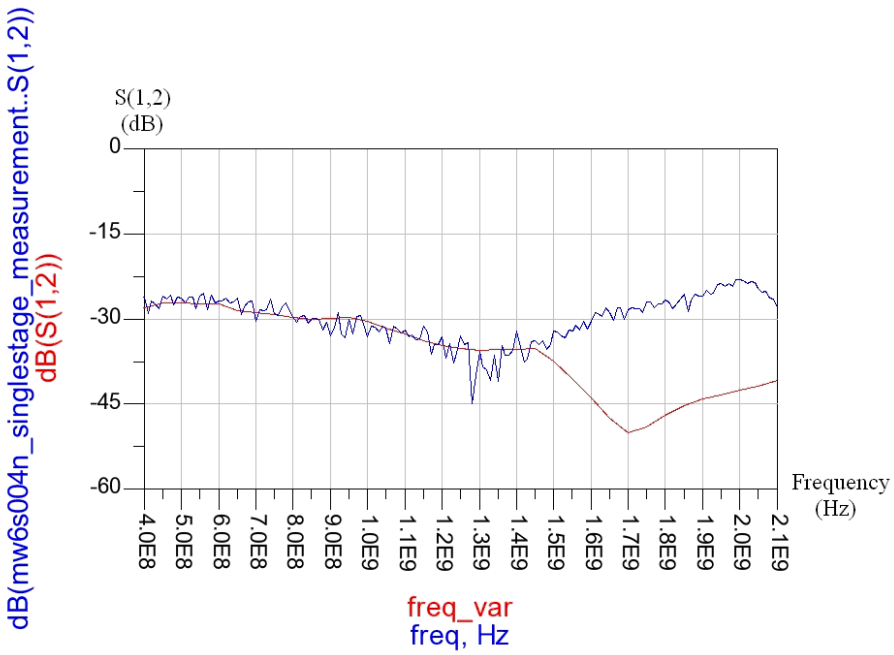

Figure 4.53: Comparison of LSSP result of S_{12} between simulation and measurement for driver stage configuration

As seen from the above graphs, the large signal s-parameter results of S21, S11, S22 and S12 from the Network Analyzer (N.A.) and Advanced Design System (ADS) are so close to each other. It seems that the power amplifier circuitry is completely modeled in simulation according to the results of the measurement. The reason of getting S22 result worse at the end of the band is; the output of the driver transistor is directly connected to 50 ohm termination in simulation and also in measurement analysis. There isn't any matching network used between the driver stage and the last stage (inter stage matching network) so we have to connect the output of the driver transistor to 50 ohm termination without any matching network.

4.3.5.3. INTERMODULATION DISTORTION

The simulated and measured IMD values are given in the table at frequencies 500MHz, 1000MHz, 1500MHz, 2000MHz.

Table 4.2: Comparison of IMD result between simulation and measurement for driver stage configuration

Frequency(MHz)	Simulation(dBc)	Measurement(dBc)
500	-35	-38,5
1000	-29,5	-33,6
1500	-31,1	-32,7
2000	-31,7	-31,9

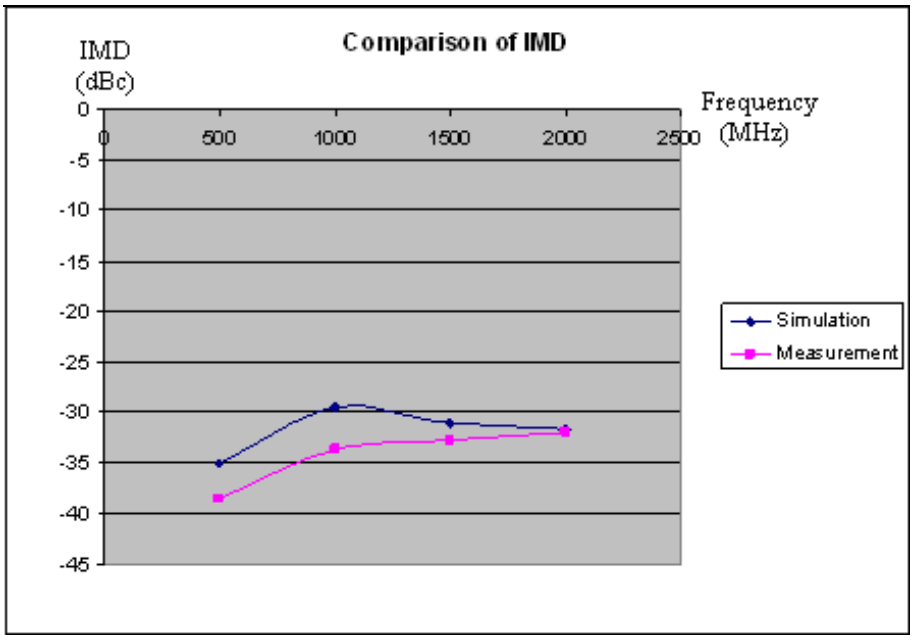

Figure 4.54: Comparison of IMD result between simulation and measurement for driver stage configuration

The above graph shows that IMD values taken from simulation and measurement processes are so close to each other.

4.4. SUMMARY

In this section we analyzed the driver stage of the power amplifier. In this project, we choose LDMOS transistor technology and the reason of choosing this technology was mentioned in previous chapter.

There is no inter circuit matching network used between the driver and the last stage. Because, the driver stage transistor output impedance is not so unfamiliar to last stage transistor's input impedance, so simplicity of the overall network, any matching network isn't put between two stages.

Parasitic effects of the system are tried to model in the simulation. In this process, the models of the lumped components are used in simulation and pad parasitics of them are tried to analyze. The ground area at the bottom side of the RF Choke pads and the transistor drain pad are removed to reduce the parasitic effects.

The comparison of simulation and measurement results can be seen in previous section, and it can be said that the simulation is properly modeled according to the results of measurement.

CHAPTER V

MULTI STAGE DESIGN OF FREESCALE MW6S004NT1 & NXP BLF3G21-6 TRANSISTORS

5.1. INTRODUCTION

This section presents modeling and analysis of the last stage of 500MHz-2000MHz broadband power amplifier. We used LDMOS RF transistor, in driver stage configuration. In last stage, we choose LDMOS RF transistor too. We decide to use NXP Company's BLF3G21-6 LDMOS transistor, after searching the whole transistor companies. For ADS simulation, the large signal model of the transistor is obtained from NXP Company.

The same procedure in driver stage amplifier design is followed. Simulations are done with components' model and model of parasitic effects according to the results of measurements. The length and width of microstrip lines and open circuit stubs in output matching network are optimized to obtain the best return loss at the whole band.

The models of the lumped components are put in simulation and pad parasitics of them are tried to analyze. The ground area at the bottom side of the RF Choke pads and the transistor drain pad are removed to reduce the parasitic effects.

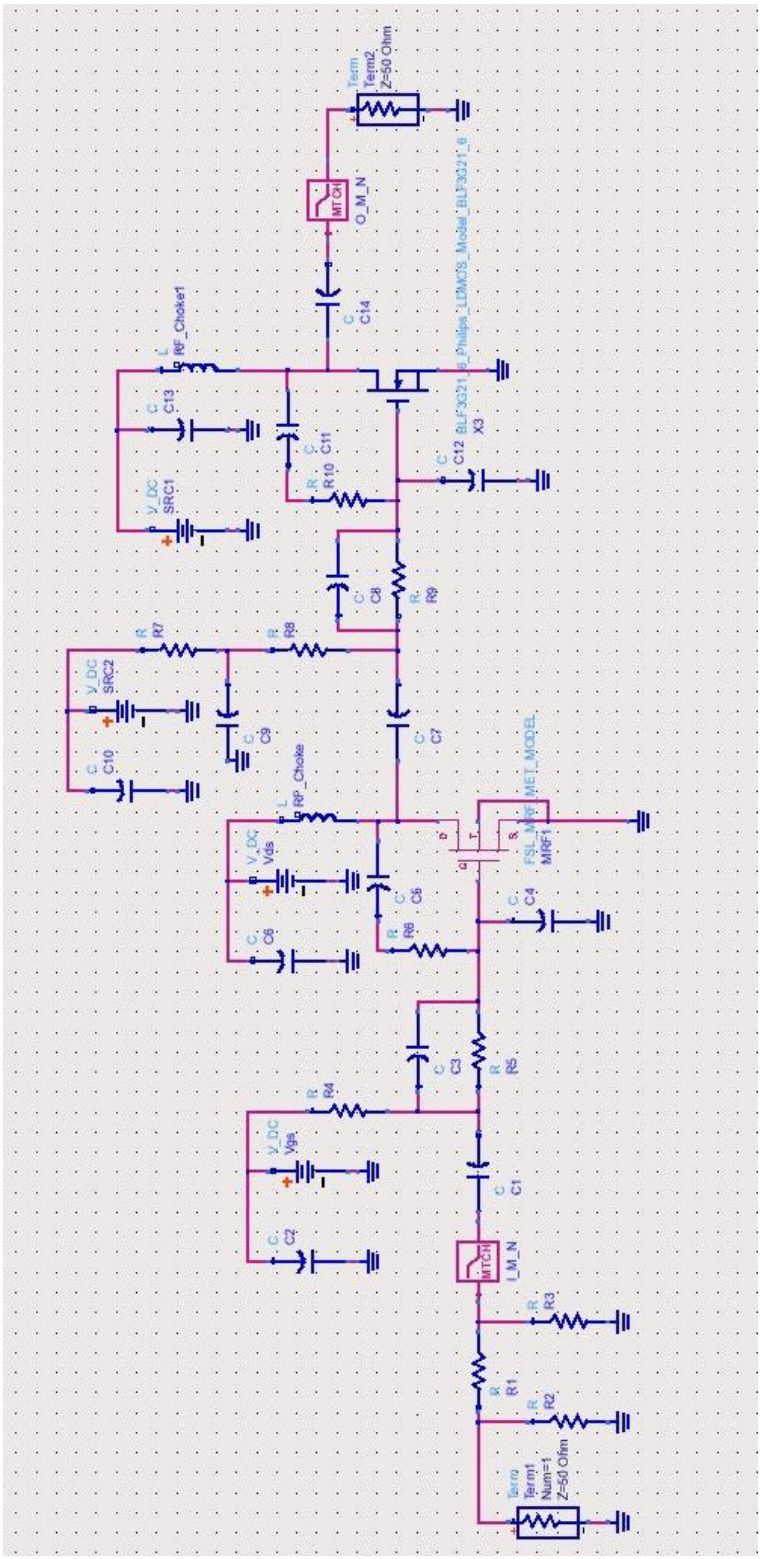

Figure 5.1: Schematic of the complete system

In multi stage design process, the configuration that is showed in Figure 5.1 is used. If we look at the last stage, for stability of the transistor, the series resistor (R9), shunt resistors (R7 and R8), and the feedback resistor (R10) are optimized. As told before, there is no matching network used between the two stages. The RF-choke is used to isolate the RF transmission line from the DC source. It is important that RF Choke has a feature that can support to pass enough DC current through the transistor. I will deeply mention the design processes of the multistage amplifier in the following sections.

5.2. CRITERIAS OF CHOSING NXP BLF3G21-6 TRANSISTOR

LDMOS technology has been chosen to design the power amplifier, as mentioned before. During the searching process of the last stage RF transistor, some problems appeared. There isn't any transistor which has large signal ADS model, and the ability of producing high output power (≥10W), and also working at broadband (500MHz-2000MHz). Power amplifier companies publish the models of transistors in two ways.

i. They publish small signal s-parameter files for different biasing conditions. If we think an RF power amplifier transistor that produces high RF power, the transistor load line enters into non-linear region in $I_d - V_{ds}$ curves, so when producing high RF power at the last stage, the transistor cannot behave like a linear component. Small signal s-parameter models aren't useful for RF power amplifier designer, because when a designer simulates the circuitry at high power level by using small signal s-parameter model for the RF transistor, the result does not make any sense for him. It is very important to have a large signal model for an RF power amplifier transistor. As a result, because the last stage transistor is pushed into

non-linear region, small signal s-parameter values of the transistor aren't suitable for us.

ii. Most of the LDMOS transistor is produced according to the need of the GSM technology, so they are useful for narrow band applications. Besides, most of them are internally matched so companies publish their model in narrow frequency band.

If LDMOS transistors are eliminated in respect of above two reasons, very few transistors left. The transistor that can work at broadband and have a large signal ADS model, and lastly can produce the highest output power, is chosen between them.

NXP Company's BLF3G21-6 transistor has LDMOS technology. According to the transistor's data sheet;

- frequency band: HF - 2200MHz
- maximum output power: 6W
- Power gain: 12.5 dB (@Pout = 7W)
- Drain efficiency: 43% (@Pout = 7W)

BLF3G21-6 has these features. From these features, it seems that this transistor can be used at the last stage in the two stage amplifier configuration.

5.3. SIMILATIONS & MEASUREMENTS

The design process of multistage amplifier begins with simulations by using ADS. Large signal model of BLF3G21-6 transistor is obtained from NXP Company. As mentioned before, there isn't any advantage to put an inter stage matching network between the driver stage and the last stage. We come this point by making some simulations with inter stage matching networks. The results of the simulations between the amplifier with an inter stage matching network and without an inter stage matching network are so close to each other. This means, the output impedance of MW6S004NT1 transistor is quite mathed to the input impedance of BLF3G21-6. Consequently, we decided to connect the driver stage to last stage without any matching network.

According to the measurement results of multi stage configuration, the lumped components and the parasitic effects are tried to model. After modeling process, it is seen that the measurement results and the simulation results are so close to each other.

5.3.1. DC BIASING

BLF3G21-6 transistor works with 28V. It is important to determine the biasing point and calculate the output impedance of the transistor to have an optimum load line swing. When DC analysis of the transistor is done in simulation, it is seen that 170 mA I_{dq} is enough for class-A operation to produce the desired output power.

Needed load impedance of the tranistor (to obtain optimum load line swing) is calculated as follows.

$$P_{LOAD} = \frac{(V_{\max} - V_{\min})(I_{\max} - I_{\min})}{8} \tag{5.1}$$

5W output power is demanded so, $P_{LOAD} = 5W$. If we think that biasing point of the transistor is 28V and to avoid the transistor from non-linear region; according to Figure 2.2, minimum value of the voltage ($V_{\min}$) must be $6V$. That means voltage can make a swing between $V_{\min} = 6V$ and $V_{\max} = 28V + (28V - 6V) = 50V$. $I_{\min}$ is approximately 0 in class-A application.

So,

$$5W = \frac{(50V - 6V)(I_{\max} - 0)}{8} \tag{5.2}$$

$$I_{\max} = 0.9A \tag{5.3}$$

$$R_L = \frac{(V_{\max} - V_{\min})}{(I_{\max} - I_{\min})} \tag{5.4}$$

$$R_L = \frac{(50 - 6)}{(0.9 - 0)} \tag{5.5}$$

$$R_L = 48.8\Omega \tag{5.6}$$

This means that 48.8Ω output impedance is needed for optimum swing of the load line. So, there is no need to use impedance transformers to transform the output impedance of the transistor to 50Ω termination. Because the needed load impedance value is very close to 50Ω .

The graphs below show the load line of the single stage system at Pout=37dBm.

For 500MHz input signal:

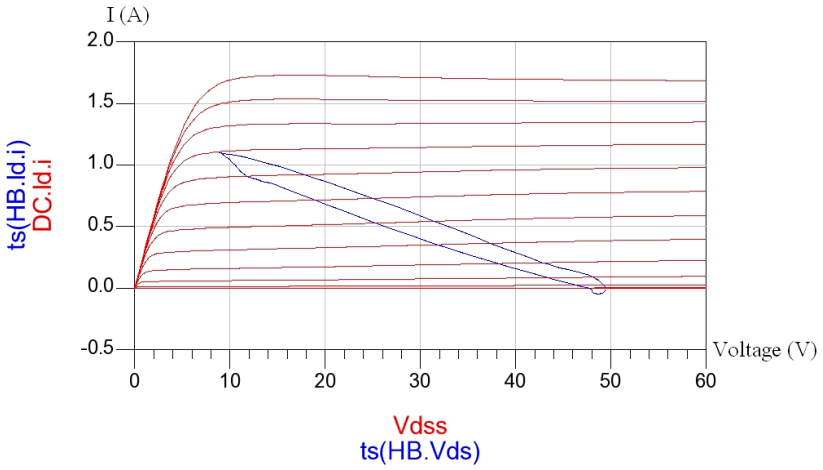

Figure 5.2: Load line in simulation at $f_c = 500MHz$

for multi stage configuration

For 1000MHz input signal:

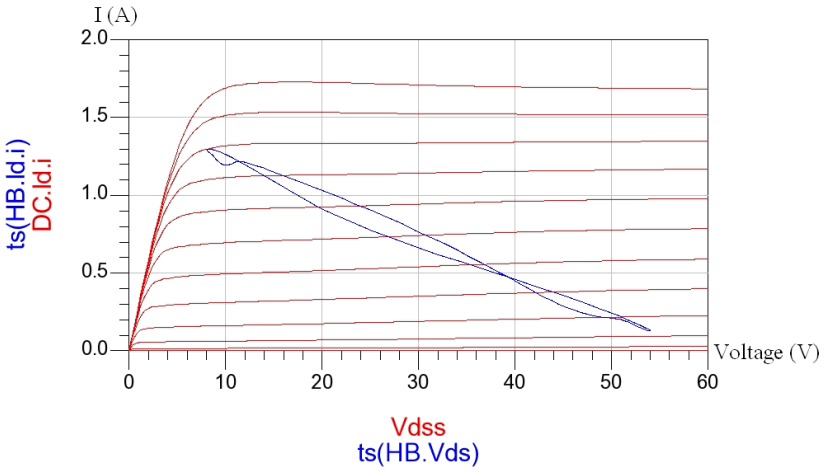

Figure 5.3: Load line in simulation at $f_c = 1000MHz$

for multi stage configuration

For 1500MHz input signal:

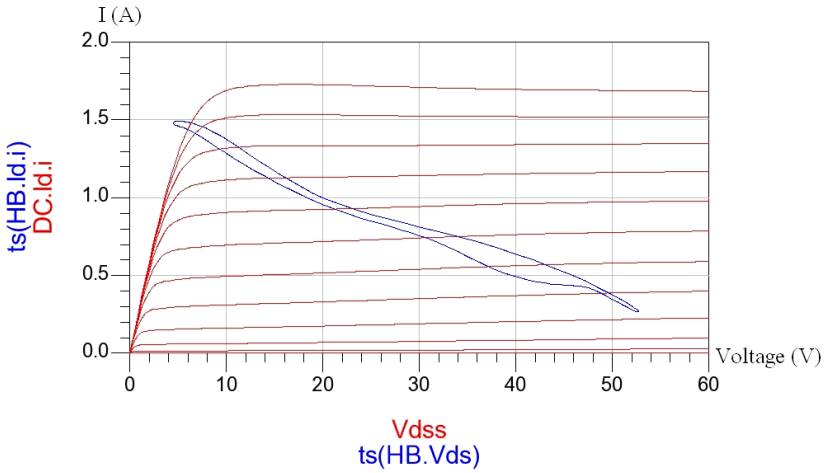

Figure 5.4: Load line in simulation at $f_c = 1500MHz$

for multi stage configuration

For 2000MHz input signal:

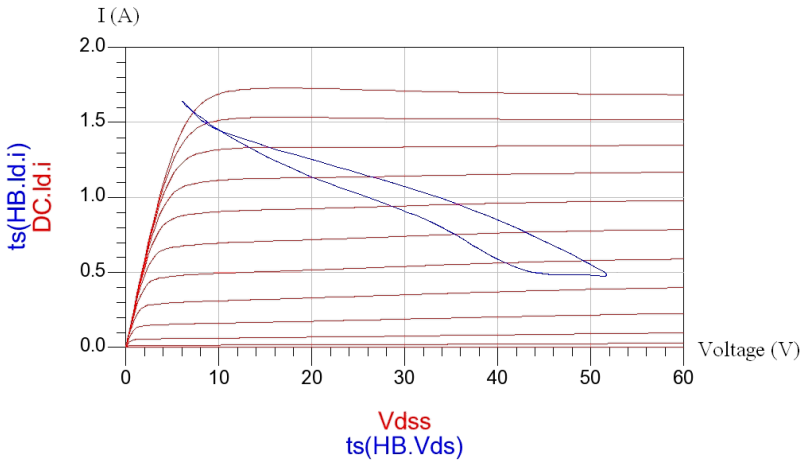

Figure 5.5: Load line in simulation at $fc = 2000MHz$

for multi stage configuration

5.3.2. DC BIASING NETWORK (DESIGN OF CHOKE)

Same configuration in driver stage is used here. When the needed DC current (Irms) is thought, Coilcraft Midi Spring Air Core Inductors of 22nH and Mini Spring Air Core Inductors of A03T (8nH) can support the required DC current.

5.3.3. SIMULATION METHODS

5.3.3.1. MODEL VERIFING

We cannot verify the model of BLF3G21-6 transistor, because the s-parameters of this transistor aren't indicated in its data sheet, so there isn't any s-parameter values to compare the model of this transistor.

5.3.3.2. STABILITY

Setup measurements are done simultaneously with simulations on ADS. Feedbacks are taken from the setup measurements, and then the lumped components and the parasitic effects of them are tried to be modeled in simulation. As seen from Figure 5.6, every components are modeled according to the model of their own and the parasitic effect of the components. Modeling of parasitic of pads at two side of the component can be seen at below schematic.

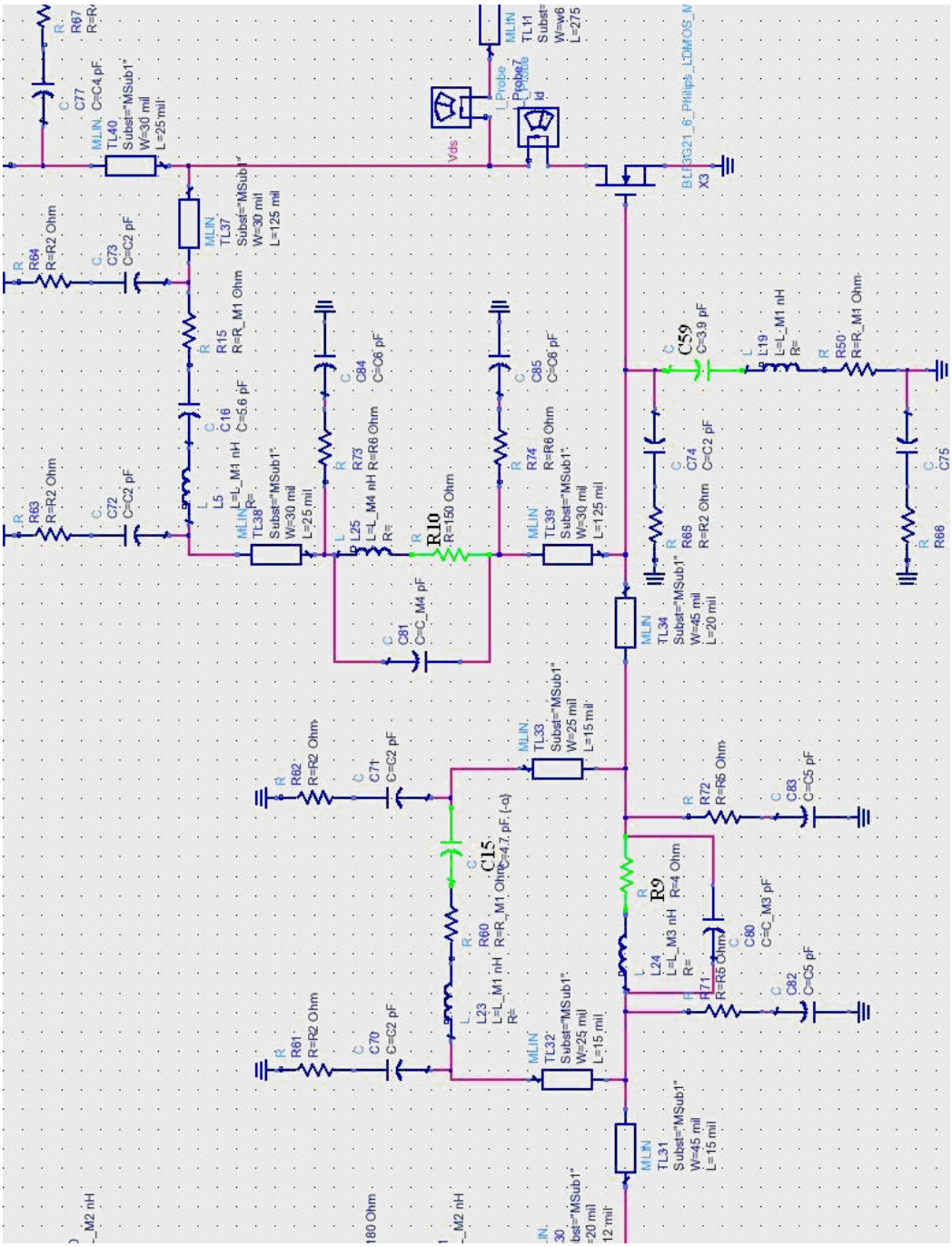

Figure 5.6: Stability analysis that show the optimized components to obtain unconditionally stable case for last stage configuration

By using the feedback resistor (R10), the series gate resistor (R9), and the parallel capacitor (C15), which optimize the gain at high frequencies, over the series gate resistor; in addition, the capacitor (C59) between the gate and the ground that improves the matching and S21; are modeled in simulation. Stability Factor (K) and Stability Measure (B) values are observed on ADS.

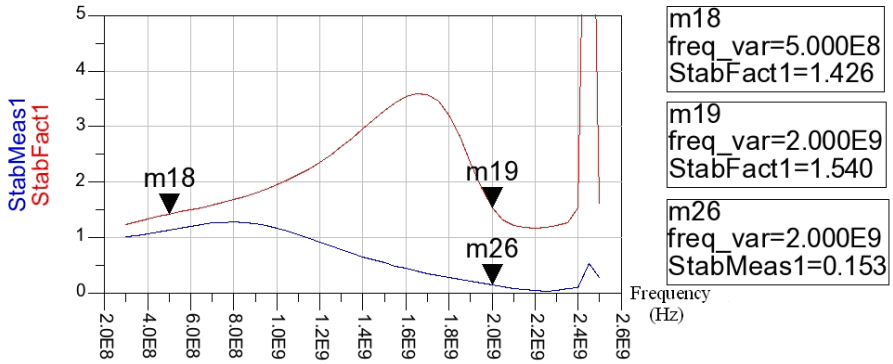

Figure 5.7: Graphs of Stability Factor (K) and Stability Measure (B) for last stage

As seen from Figure 5.7, the circuitry behaves as stable (Stability Factor>1 and Stability Measure>0).

5.3.3.3. SCATTERING PARAMETERS

If we look at the multistage configuration after modeling the component in simulation according to the measurement results, the graphs below which show the Large Signal S-Parameters, are taken. In LSSP simulation, 33 dBm output power is aimed at the whole band.

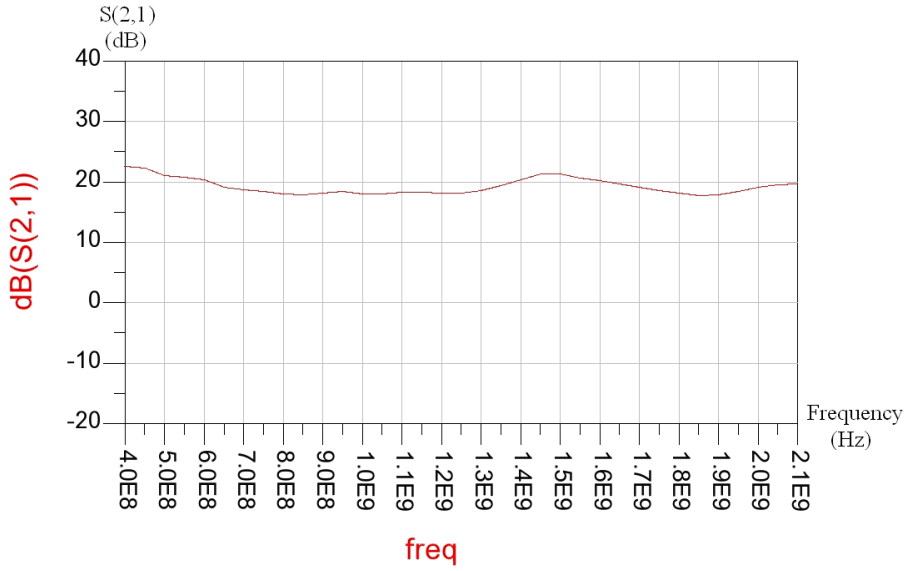

Figure 5.8: The simulation result of LSSP of S_{21} for multi stage configuration

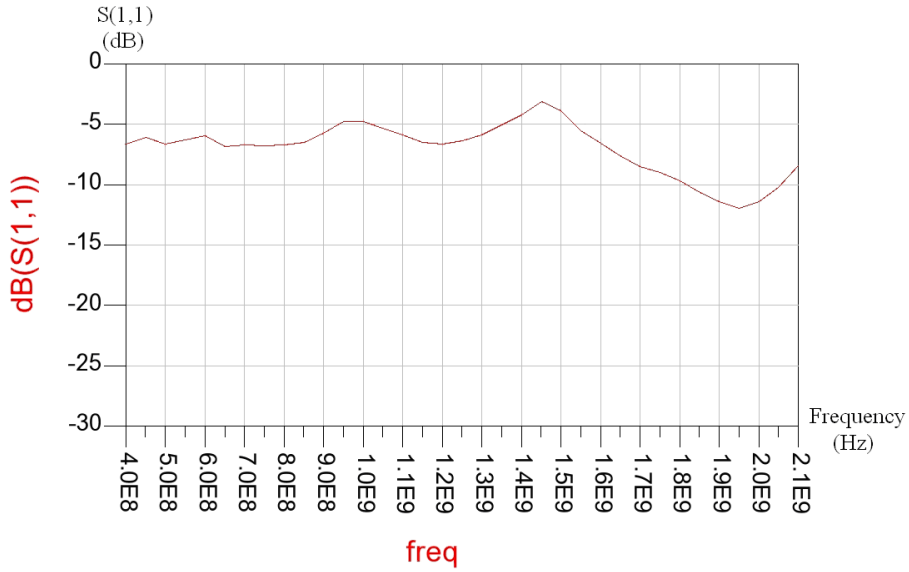

Figure 5.9: The simulation result of LSSP of S_{11} for multi stage configuration

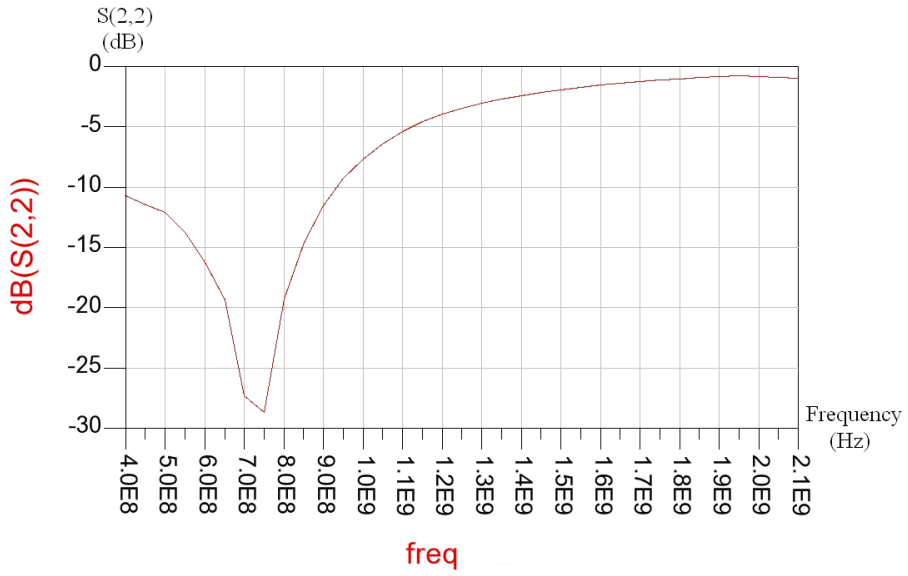

Figure 5.10: The simulation result of LSSP of S_{22} for multi stage configuration

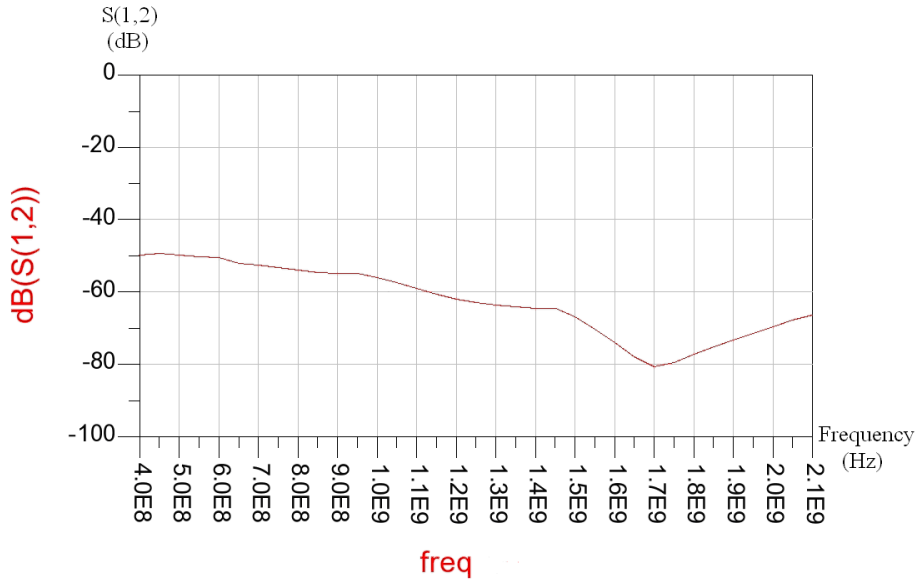

Figure 5.11: The simulation result of LSSP of S_{12} for multi stage configuration

These LSSP values are taken when the output power is 33 dBm. To see the non-linear effects of the BLF3G21-6 transistor, it is important to make the simulation

whereas producing high output power. As seen from Figure 5.8, the gain of the multistage configuration is flat at whole band. But it is more important to produce the demanded power at the whole band, rather than having a flat gain at the whole band.

The input matching network values (that is the length and the width of the microstrip lines and open circuit stubs) that are taken from the simulation seemed compatible to measurement results. But, it cannot be said for output matching network. The length and width values of microstrip lines and open circuit stubs of the output matching network that are taken from the simulation didn't make the output return loss well in measurement process. The simulation and the measurement results did not match each other. We thought that the model of BLF3G21-6 can cause this situation.

We aren't able to verify the model of BLF3G21-6 transistor, because s-parameter values isn't written in its data sheet. Although we have the ADS model of the transistor, there is no values to compare them.

To reduce the parasitic effect that arises from the last stage transistor pads, the ground area at the bottom side of the drain pad is removed. Thus, it is observed that the amplifier starts to produce more power at high frequencies, without reducing the performance at low frequencies. However this action improves the maximum output power at high frequencies of the power amplifier, removing the ground area at the bottom side of the Gate pad reduces the maximum output power at high frequencies, so the ground areas are removed only at the bottom side of the Drain pad and chokes. Furthermore, putting a shunt capacitor between the gate of the transistor and the ground improves the broadband performance of the amplifier. It is seen that, somehow, this capacitor improves the matching between the driver stage and the last stage.

5.3.3.4. MAXIMUM OUTPUT POWER

One of the main goal of this design is obtaining the highest output power at the whole band (500MHz - 2000MHz). In simulation there is no restrictions to get the highest output power, but in measurement process we have to give input power to the system under controlled. Thermal limitations can cause the transistor burn at high input power level. The graph below shows the maximum output power taken from the overall system in simulation.

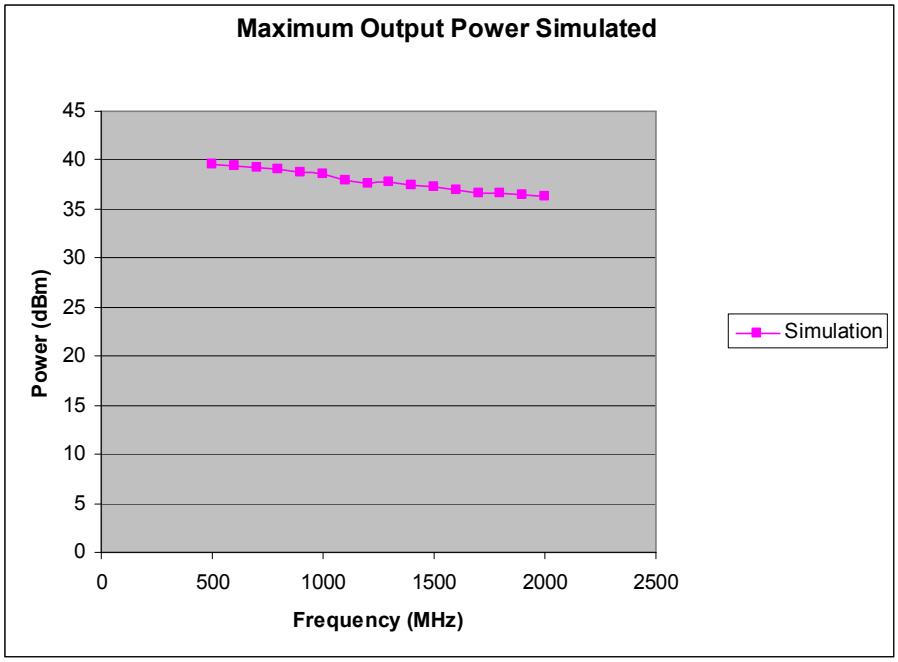

Figure 5.12: The simulation result of Maximum Output Power for multi stage configuration

It can be seen that maximum output power decreases at high frequencies. This situation is expected in design process of a power amplifier, maximum output power that an amplifier can produce usually decreases at high frequencies. I will compare this simulated results with measured ones later.

5.3.3.5. INTERMODULATION DISTORTION

The simulation of IMD is done with two equal power input signals and there is 1 MHz difference between them. In simulation, the output power of the multi stage configuration is arranged to 33dBm (2W). Two equal power signals are given to the system, so Peak Envelope Power (PEP) of these two signals has to be 33dBm. The PEP is assumed to be twice the RMS power indicated, ignoring the harmonic content of the output signal [25]. If the voltage level of single tone is assumed to be V then the voltage level of each one of these two tones have to be $V/2$. As known, power is related to square of voltage. As a result, power levels of these to signal have to be 4 times (6dB) lower than power level of single tone. Following figures show IMD results at different frequencies.

$fc1 = 500MHz, fc2 = 501MHz$:

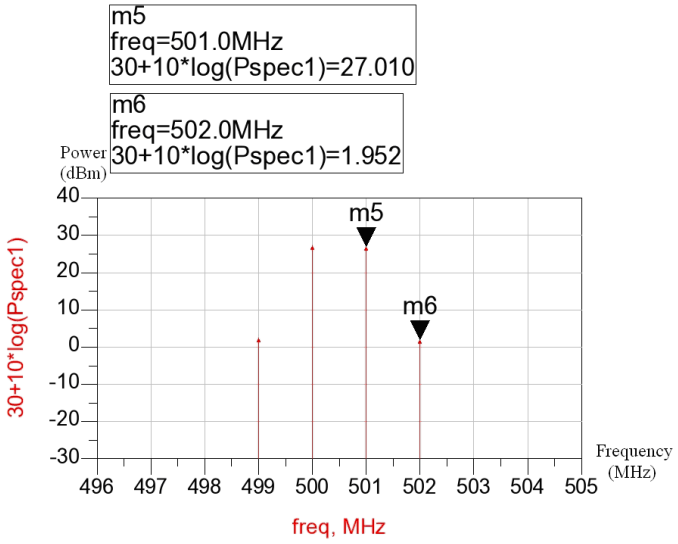

Figure 5.13: The simulation result of IMD at 500MHz for multi stage configuration

$fc1 = 1000MHz, fc2 = 1001MHz$:

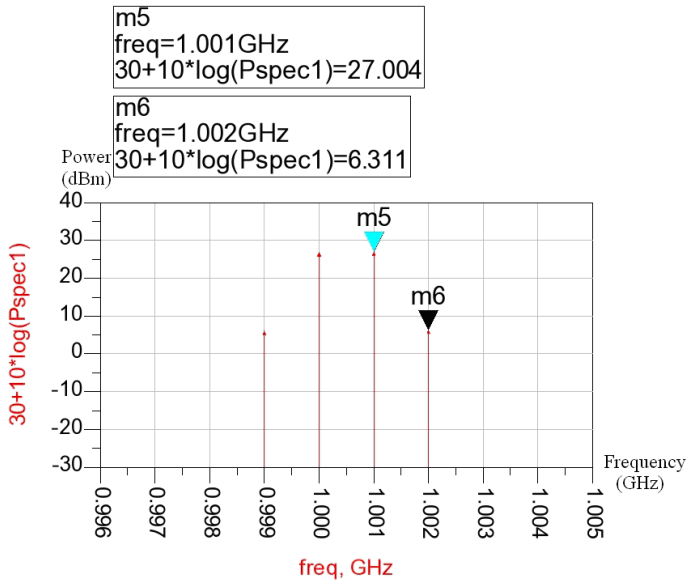

Figure 5.14: The simulation result of IMD at 1000MHz for multi stage configuration

$fc1 = 1500MHz, fc2 = 1501MHz$:

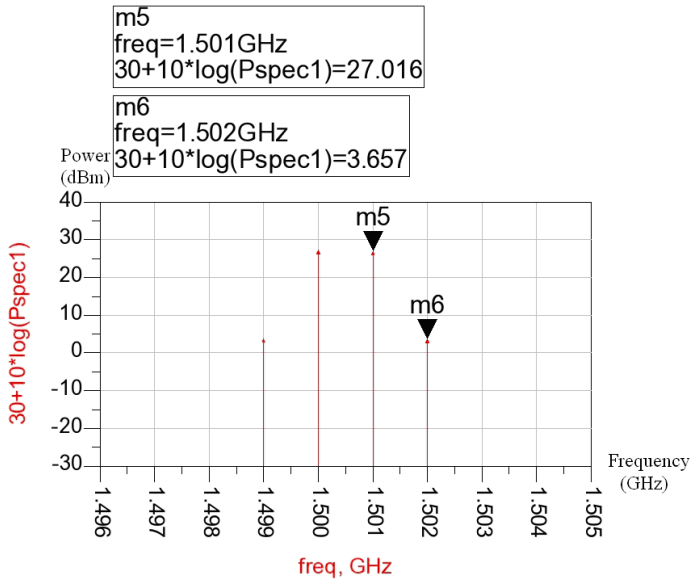

Figure 5.15: The simulation result of IMD at 1500MHz for multi stage configuration

$fc1 = 2000MHz, fc2 = 2001MHz$:

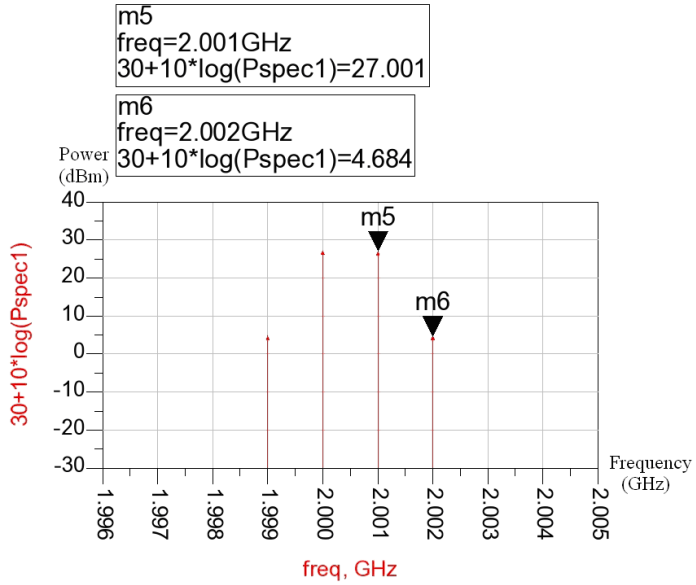

Figure 5.16: The simulation result of IMD at 2000MHz for multi stage configuration

As seen from the above figures, the IMD value of the multi stage system is simulated as -21dBc at worst case.

These results seemed to be poor. In cascaded systems, IMD characteristic of driver stage can influence the performance of the complete system.

Most linear amplifiers (i.e. class-A and class-AB) consist of a cascade of two or more amplifier stages. The overall distortion is mainly caused by the final stage because the driver stages are generally designed to have a lower distortion. In fact, attention to the design of the driver stage will pay dividends in overall performance as the following analysis illustrates.

The total distortion of a multi-stage amplifier, d_{tot}, can be determined from:

$$d_{tot} = 20\log\left(10^{d1/20} + 10^{d2/20} + \ldots\right) \tag{5.7}$$

where d_1, d_2 etc. are the intermodulation products of each stage in dB.

With two stages, e.g. driver plus a final stage, it is useful to know by how many dB the overall distortion worsens for a given difference in distortion between driver and final stage (assuming the driver distortion is the smaller). This relationship is described by:

$$B = 20\log\left(1 + 10^{-A/20}\right) \tag{5.8}$$

where:
A is the absolute difference in distortion between driver and final stage, and
B is the increase in distortion in the output of the amplifier.

This relationship is summarized in Table 5.1 for a few values. Clearly, if a large increase in distortion is unacceptable, the driver stage has to be substantially better than the final stage [26].

Table 5.1: Effects of driver distortion upon overall distortion

A Amount by which driver IMD is superior to final stage IMD (dB)	**B** Increase in IMD of output amp. (dB)
0	6.0
5	3.9
10	2.4
15	1.4
20	0.8

In our design the IMD value of the driver stage can be thought as approximately -30dBc at worst case. If we think that the last stage IMD value at worst case is same as the driver stage's, the overall system IMD value can be 6dB worse, as compare to last stage. I mean that, the overall system has -24dBc IMD result at worst case.

As a result, it is impotant to decrase the IMD value of driver stage to get low IMD characteristic in overall system.

5.3.3.6. EFFICIENCY

As mentioned before, most of the LDMOS transistor is produced according to the need of the GSM technology, so they are useful for narrow band applications. There are very few LDMOS transistors that are suitable for broadband applications. For narrow band applications, it is possible to design an amplifier that can produce high output power with high gain, high efficiency and high linearity. The broadness of the frequency band causes to reduce the transistor output matching performance especially at high frequencies.

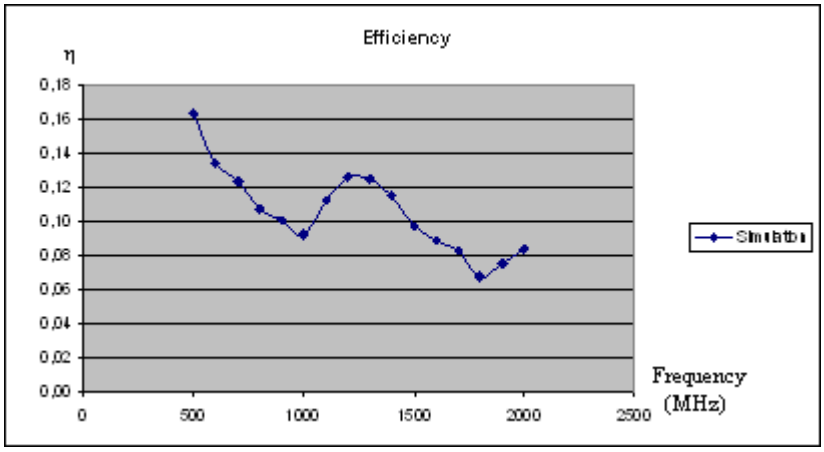

Figure 5.17: The simulation result of Efficiency for multi stage configuration

If we look at the output impedance of BLF3G21-6 transistor on Smith Chart, we can see that the imoedance is scattered too much at broadband. Especially at higher frequencies, we can observe that the output impedance of the transistor decreases a lot.

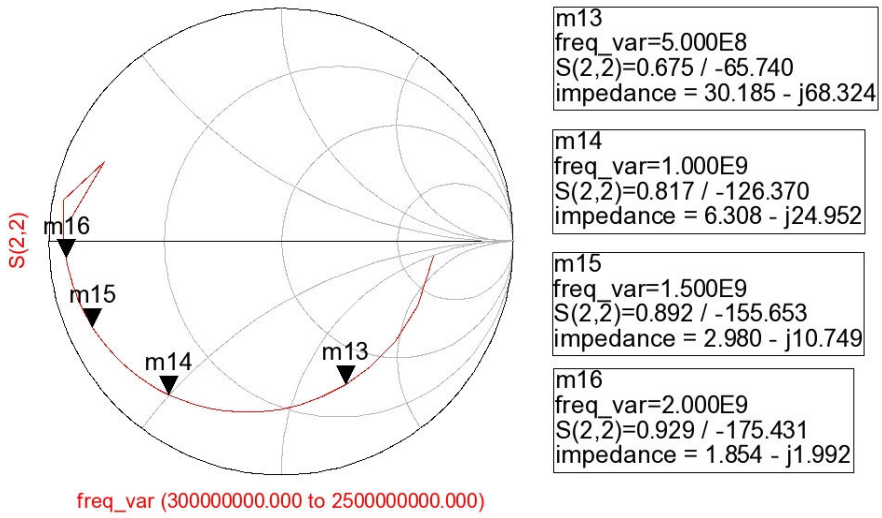

Figure 5.18: Output impedance of BLF3G21-6 at broadband

If we think that, the termination point at the output of the transistor is 50 ohm, it is very hard to match the transistor, because its output impedance is scattered too much, and it has very low output impedance at higher frequencies. The output return loss is tried to improve, and the best output matching configuration is tried to find.

5.3.3.7. 1dB COMPRESSION POINT

The following graph shows the compression point of the multi stage amplifier configuration where the input signal frequency is 1.5GHz.

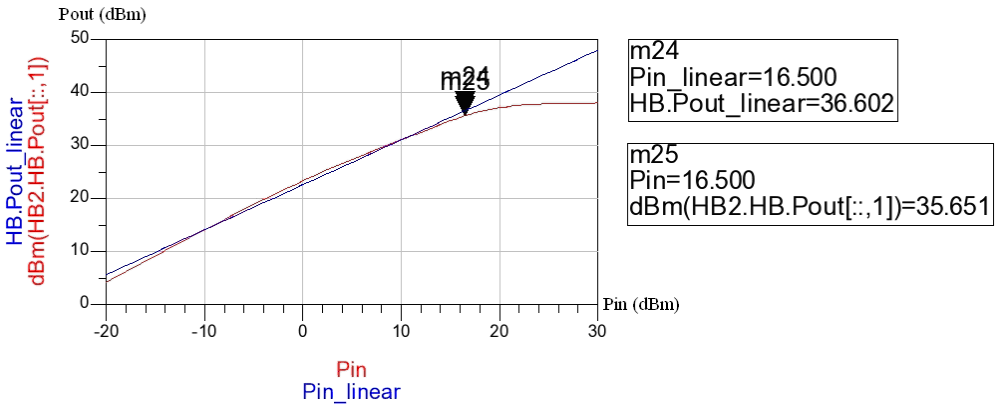

Figure 5.19: The simulation result of 1dB Compression Point for multi stage configuration

From Figure 5.19 it can be seen that 1dB compression point of the multi stage amplifier configuration is approximately 35.6dBm. Whether it looks early to enter in compression region, the poorness of S22 values at frequencies above 1.5 GHz can cause this.

5.3.4. MEASUREMENT METHODS

5.3.4.1. STABILITY

The last stage transistor behaves as stable by using the feedback components which are found in simulation. There isn't any oscillation occurred during the measurement process.

5.3.4.2. SCATTERING PARAMETERS

Scattering parameters of the multistage amplifier configuration are measured at below setup.

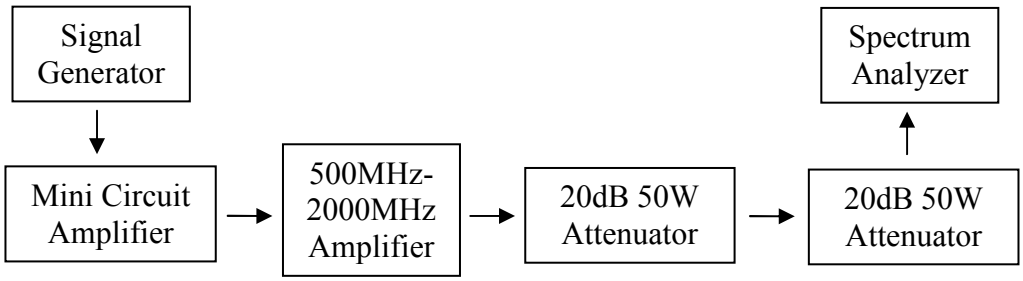

Figure 5.20: Setup is established to measure large signal s-parameter of S_{21} for multi stage configuration

Large signal gain of the overall system is measured only by using the above setup. For measuring the input and output return losses, it is needed to use a network analyzer as we did in driver stage section. But, when the scattering parameters of the driver stage was measured, the output power was low. There is one more section added to driver stage, and then the output power of the system gets high, so we have to put larger (i.e. 40dB) attenuators to protect the network analyzer. When we put larger attenuators in setup, the network analyzer isn't able to measure the input and

output impedances of the system, because the input and output impedances of the system are low, and with respect to network analyzer they exist behind the attenuators. Measuring low impedances behind the attenuators is very difficult. Network analyzer isn't able to measure these impedances after large attenuator. They are designed to measure small signal s-parameters. In a conclusion, spectrum analyzer is used to measure only large signal gain at Pout=33dBm at the whole band. The output power is adjusted to 33dBm by tuning the input signal level at he whole band.

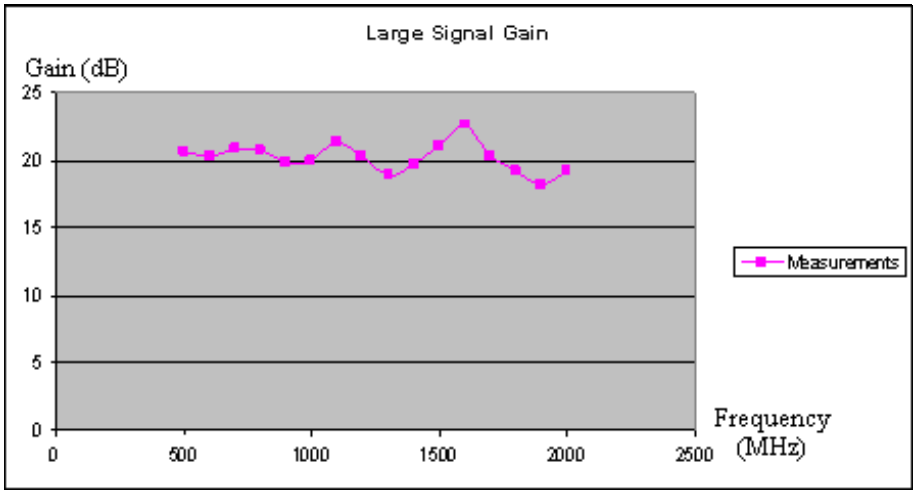

Figure 5.21: The measurement result of LSSP of S_{21} for multi stage configuration

When the above figure is analyzed, it is important to remember the measuring tolerances. It can be said that it is possible to have ±1dB tolerance when we measure the large signal gain of the system.

5.3.4.3. MAXIMUM OUTPUT POWER

However we had aimed to produce 5W output power at the whole band with multistage configuration; due to the last stage transistor has 6W maximum output

power; and also input and output impedances of LDMOS transistors are scattered too much (input and output return losses cannot be improved too much) at broadband applications, we aren't able to produce 5W output power at the whole band. At high frequencies, because of getting the output return loss worse, the maximum output power of the system is decreasing.

Figure 5.22 shows the maximum power that is taken from the amplifier, with respect to frequency.

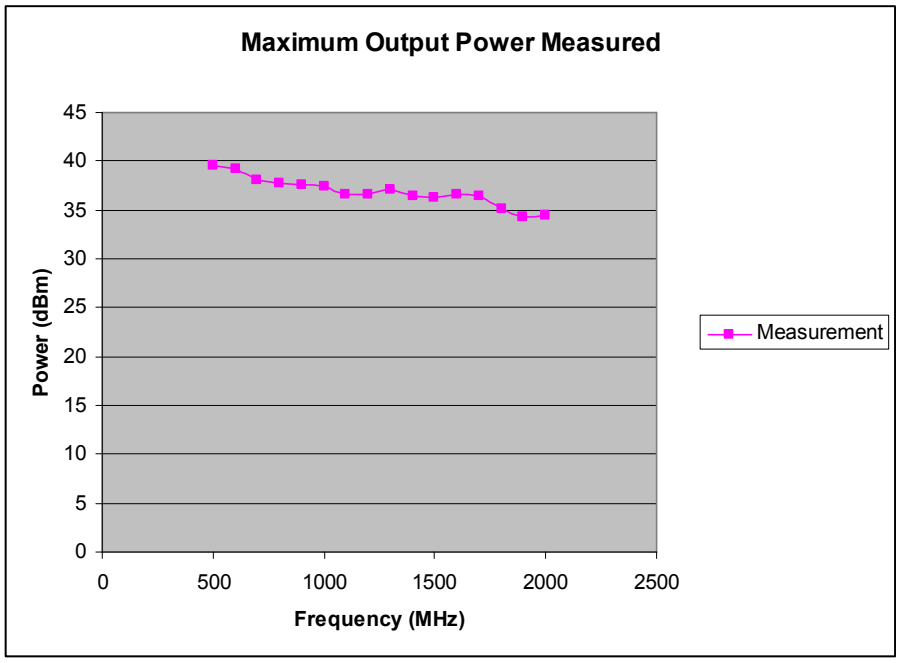

Figure 5.22: The measurement result of maximum output power taken from the complete amplifier system

Input and output matching networks of the multistage configuration are simulated by using ADS Large Signal S-Parameter tool in Harmonic Balance Simulation when output power is 37 dBm at whole band, and then the length and width values of microstrip lines and open circuit stubs are found by optimizing input and output return losses in simulation.

The values that are found from the simulation for input matching network, gave the same results at measurements on the board. But, it cannot be said for output matching network, so the output matching network is tried to matched by tuning the length and width of microstrip lines and open circuit stubs on printed circuit board. Before this process, the amplifier was able to produce 37 dBm output power up to 1.5 GHz, but the frequencies between 1.5GHz and 2 GHz the maximum output power reduced dramatically. The maximum output power is tried to make flat at whole band by modifying the output matching network.

Figure 5.23 shows the maximum output power with respect to frequency and compares the results of before optimization and after optimization processes.

Table 5.2: The result of maximum output power in comparison between before and after optimization of output matching network

Frequency (MHz)	Maximum Output Power Before Optimization (dBm)	Maximum Output Power After Optimization (dBm)
500	39,20	39,50
600	38,50	39,20
700	37,60	38,10
800	37,60	37,70
900	37,70	37,65
1000	38,00	37,50
1100	38,70	36,60
1200	39,00	36,55
1300	38,50	37,10
1400	37,50	36,40
1500	36,20	36,20
1600	34,20	36,60
1700	31,60	36,50
1800	30,50	35,10
1900	29,30	34,30
2000	27,00	34,40

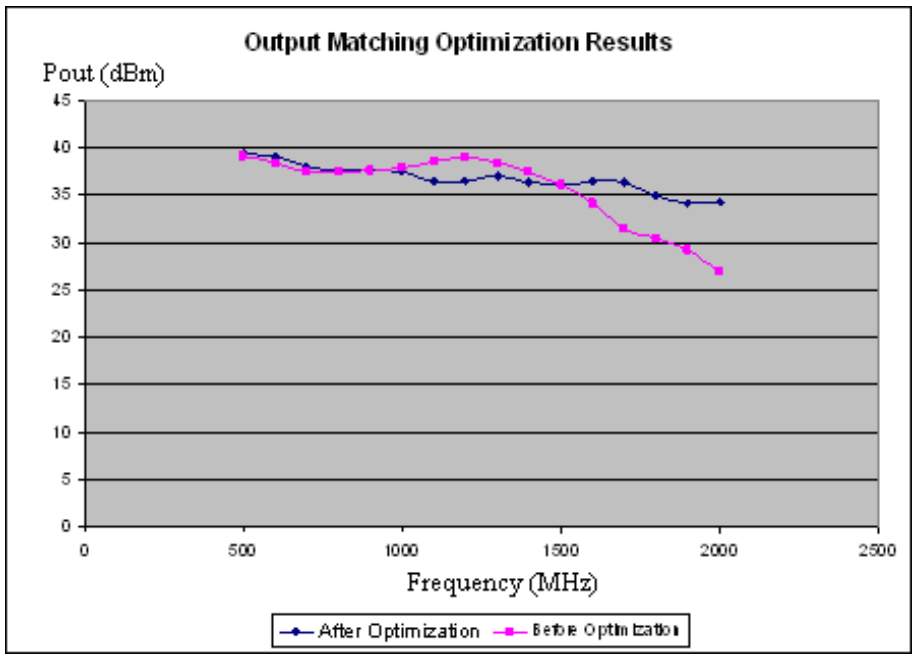

Figure 5.23: The result of maximum output power in comparison between before and after optimization of output matching network

The comparison between the maximum output power results before and after optimazion are given in the above graph. It can be seen that the maximum output power gets flat at the whole band after modifing the output matching network. In Table 5.2 it can be seen that the maximum output power dramatically reduced at 2000MHz before optimization process. By modifing the output mathing network the maximum output power increases without reducing the performance too much at lower frequencies.

5.3.4.4. INTERMODULATION DISTORTION

The setup below is established to measure IMD of the multi stage configuration.

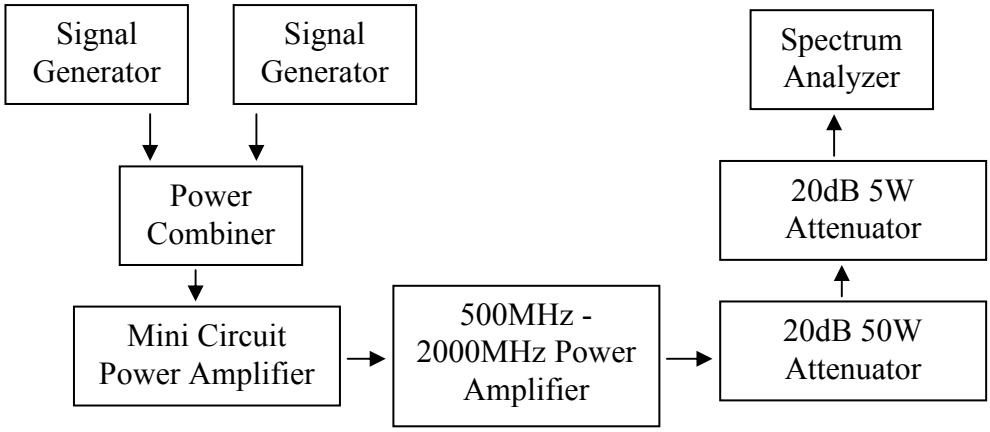

Figure 5.24: Setup is established to measure IMD of multi stage configuration

According to the above setup, two equal power input signals are generated by two signal generators, and they are summed in Power Combiner, then Mini Circuit Power Amplifier amplifies the summed signal to demanded input level of 500MHz-2000MHz Power Amplifier. This amplifier amplifies the summed input signal to 33dBm Peak Envelope Power, and then two attenuators attenuate this summed signal, finally IMD can be measured in the Spectrum Analyzer.

The IMD of Mini Circuit Power Amplifier is measured as -50dBc. So, it can be said that this amplifier doesn't influence the IMD value of 500MHz-2000MHz Power Amplifier, because its IMD value is too low.The results of IMD are given below for 500MHz, 1000MHz, 1500MHz, and 2000MHz at 33dBm Peak Envelope Power.

$fc1 = 500MHz, fc2 = 501MHz$:

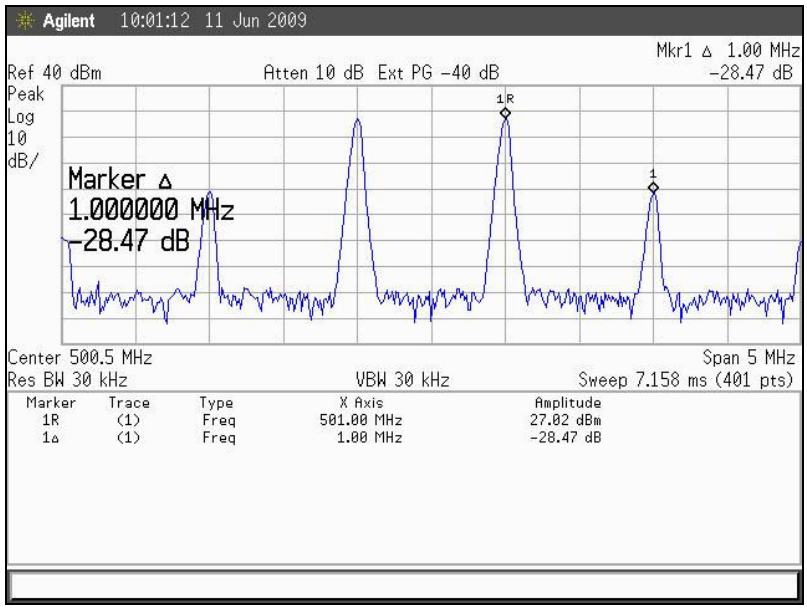

Figure 5.25: The measurement result of IMD at 500MHz for multi stage configuration

$fc1 = 1000MHz, fc2 = 1001MHz$:

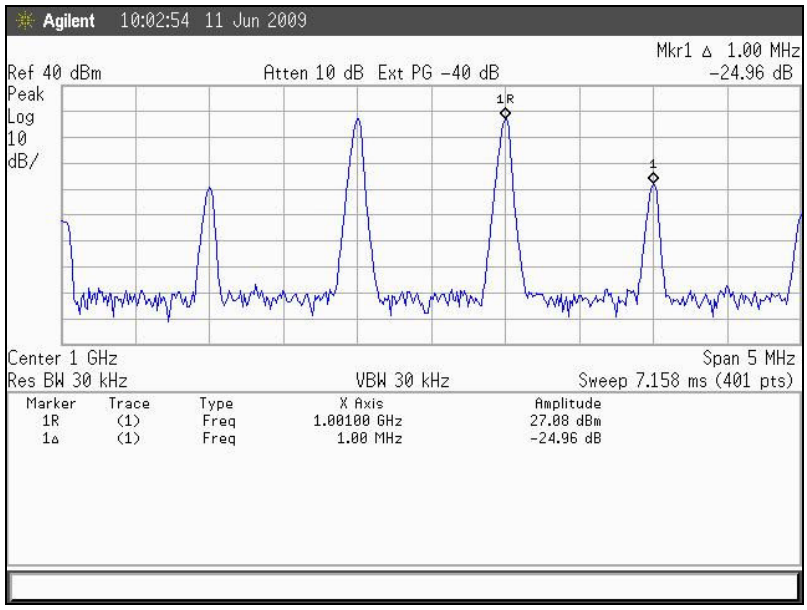

Figure 5.26: The measurement result of IMD at 1000MHz for multi stage configuration

$fc1 = 1500MHz, fc2 = 1501MHz$:

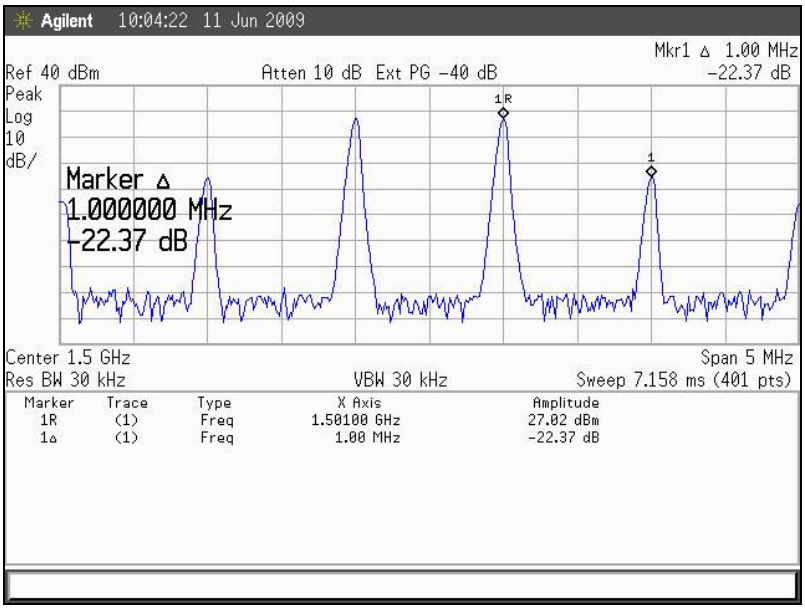

Figure 5.27: The measurement result of IMD at 1500MHz for multi stage configuration

$fc1 = 2000MHz, fc2 = 2001MHz$:

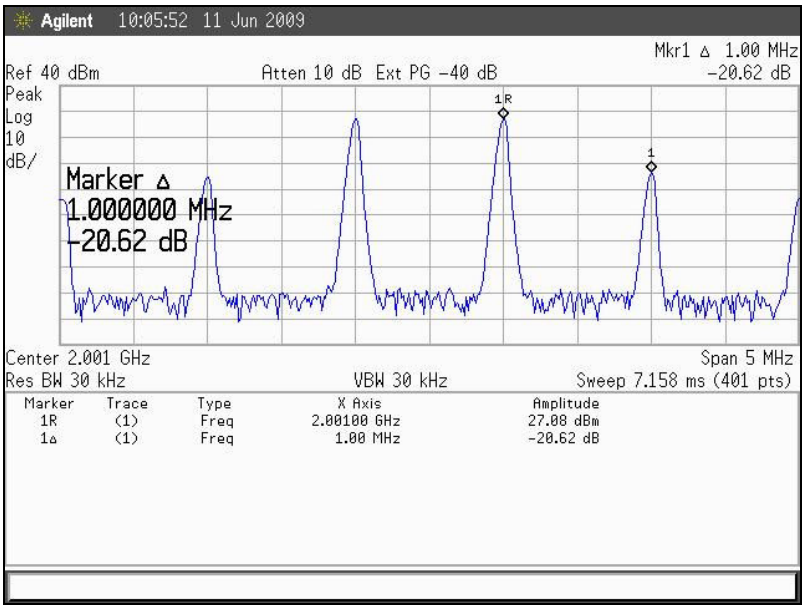

Figure 5.28: The measurement result of IMD at 2000MHz for multi stage configuration

As seen from the above graphs, the IMD at 33dBm PEP is -20.6 dBc at worst case.

5.3.4.5. EFFICIENCY

Most of the LDMOS transistor is produced according to the need of the GSM technology, so they are useful for narrow band applications, was mentioned before. In BLF3G21-6 transistor data sheet, efficiency characteristic is indicated as 43% at Pout=7W. The broadness of our frequency band causes reducing the transistor output matching performance especially at high frequencies, so it reduces the efficiency performance too.

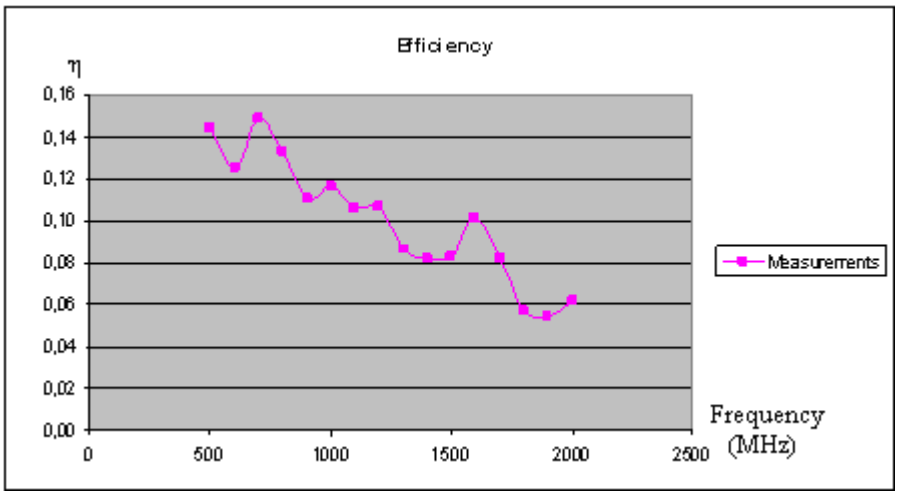

Figure 5.29: The measurement result of Efficiency for multi stage configuration

The results of efficiency performance is seen in Figure 5.29. It can be said that these results are expected, because of the transistor capabilty. 43% efficiency performance have to be obtained in narrow band application. Thus, the results at above figure is reasonable for broadband application.

5.3.4.6. Pout vs. Pin CURVES

The following graphs show the measured P_{out} vs. P_{in} curves of the multi stage amplifier configuration where the input signal frequency is 500MHz, 1000MHz, 1500MHz, and 2000MHz.

at $fc = 500MHz$:

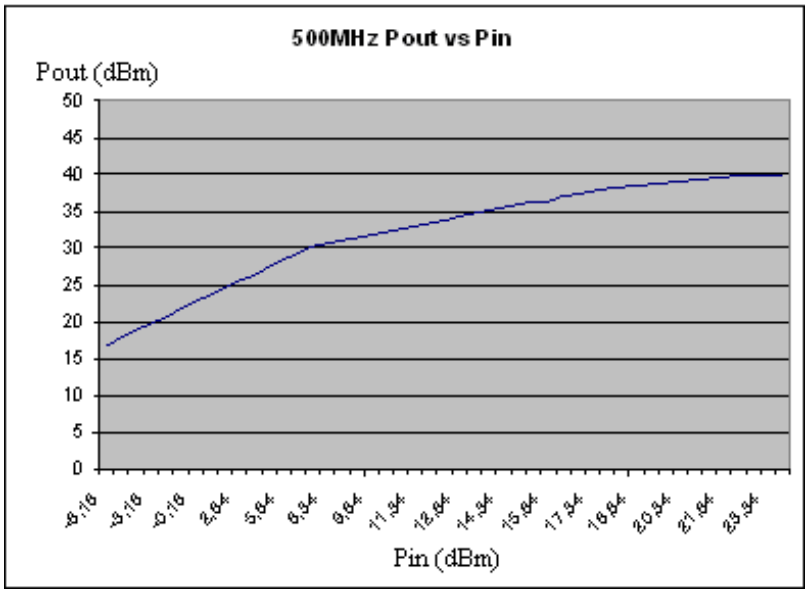

Figure 5.30: The measurement result of P_{out} vs. P_{in} curves at 500MHz for multi stage configuration

at $fc = 1000MHz$:

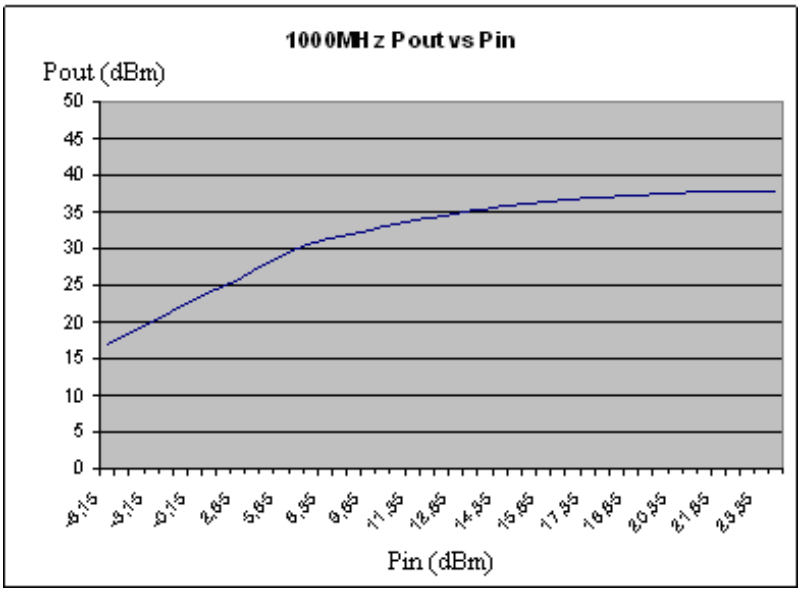

Figure 5.31: The measurement result of P_{out} vs. P_{in} curves at 1000MHz for multi stage configuration

at $fc = 1500MHz$:

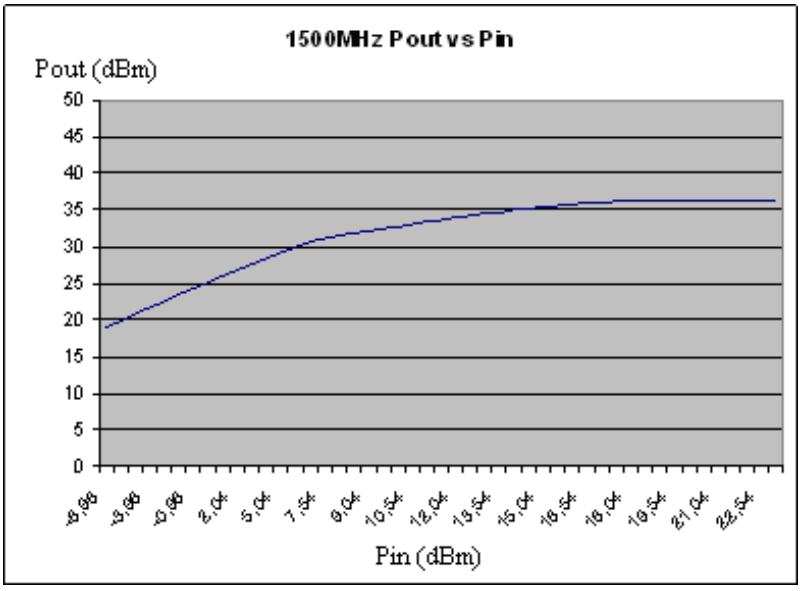

Figure 5.32: The measurement result of P_{out} vs. P_{in} curves at 1500MHz for multi stage configuration

at $fc = 2000MHz$:

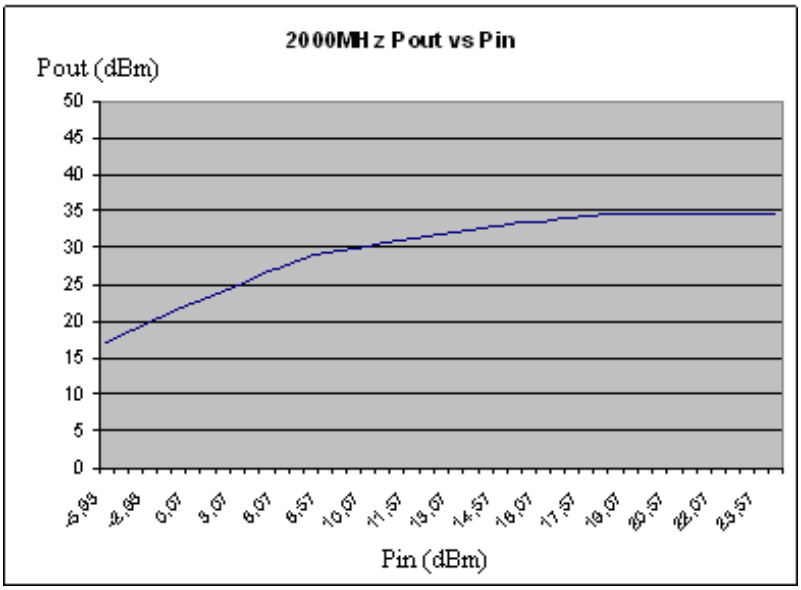

Figure 5.33: The measurement result of P_{out} vs. P_{in} curves at 2000MHz for multi stage configuration

5.3.5. COMPRESSION BETWEEN SIMULATION & MEASUREMENT RESULTS

5.3.5.1. STABILITY

To obtain the stability of the transistor, the component values which are found from the simulation, are suitable for measurements too. During the measurement process, there isn't any oscillation seen in the whole band.

5.3.5.2. SCATTERING PARAMETERS

The graph is given below that compare the large signal gain results between the simulation and the measurement. These results are taken when the output power of the complete system is 33dBm

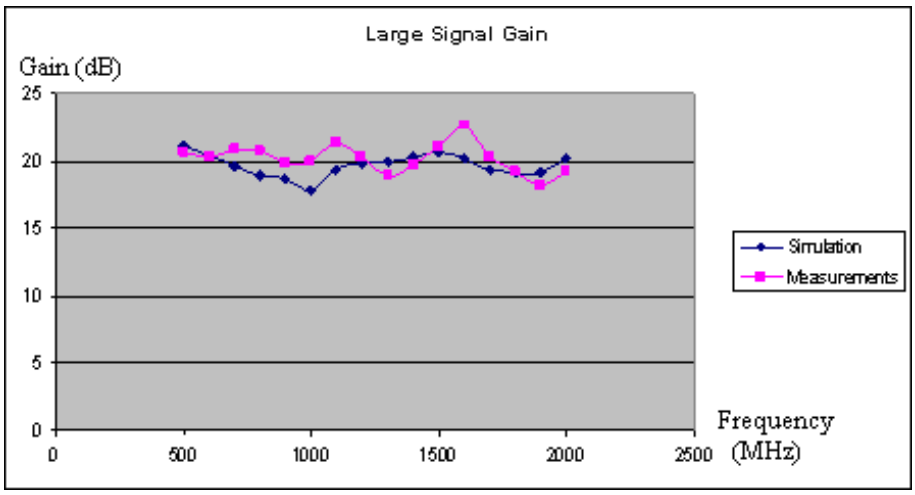

Figure 5.34: Comparison of LSSP result of S_{21} between simulation and measurement for multi stage configuration

As seen from Figure 5.34, the large signal gain results are to close to each other.

5.3.5.3. MAXIMUM OUTPUT POWER

Figure 5.35 shows the comparison of performance on maximum output power handled by the amplifier between the simulation and the measurement.

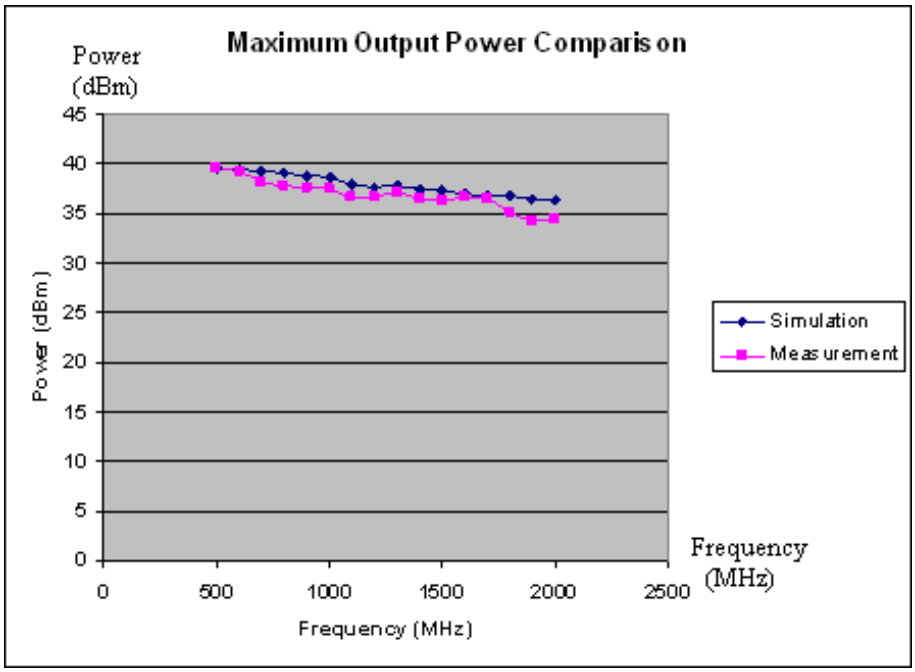

Figure 5.35: Comparison of maximum output power between simulation and measurement for multi stage configuration

5.3.5.4. INTERMODULATION DISTORTION

The IMD values are given in Table 5.3 for specific frequencies that compare the results taken from the simulation and the measurement at 33dBm output power.

Table 5.3: Comparison of IMD results between simulation and measurement for multi stage configuration

Frequency (MHz)	Simulation (dBc)	Measurement (dBc)
500	-25,058	-28,47
1000	-20,693	-24,96
1500	-23,359	-22,37
2000	-22,317	-20,62

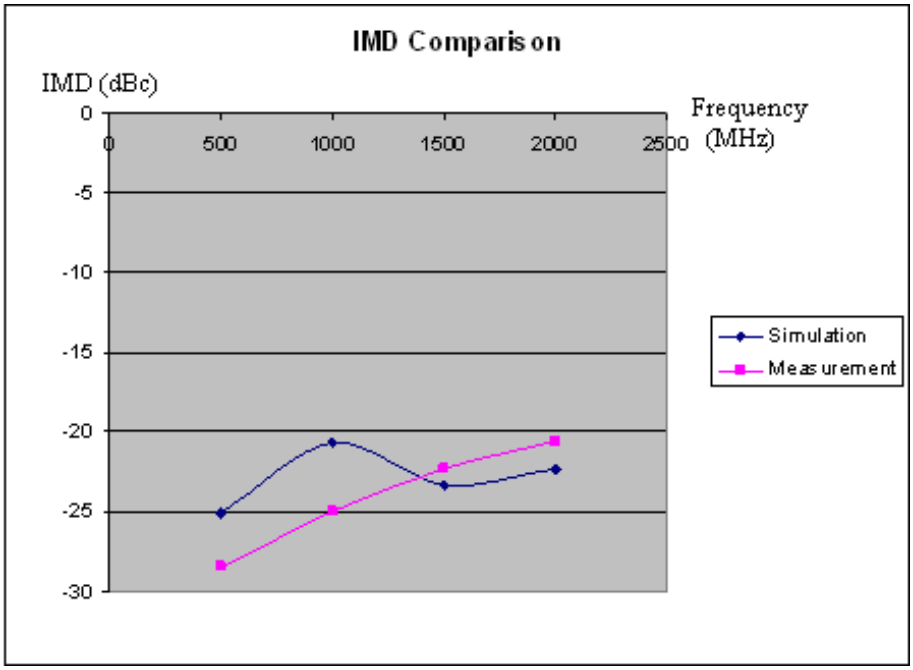

Figure 5.36: Comparison of IMD results between simulation and measurement for multi stage configuration

As seen from Figure 5.36, the results are very close to each other. The worseness of IMD of the complete system is as a result of poor IMD performance of the driver stage. IMD performances of both two stages are very close to each other, so driver stage influences the IMD performance of the complete system too much.

5.3.5.5. EFFICIENCY

The information about efficiency performance of BLF3G21-6 is given in its data sheet as 43% (@Pout = 7W). If the efficiency performance of the complete system is analyzed according to the information on data sheet, it can be said that the design is successful when the efficiency criteria is considered.

In data sheet, the efficiency value of 43% is given for narrow band application which must have better return loss than our design. As a result, it's normal to get efficiency result worse than the information written in data sheet, because we try to design broadband amplifier so the input and the output return losses cannot be better than the application in data sheet has.

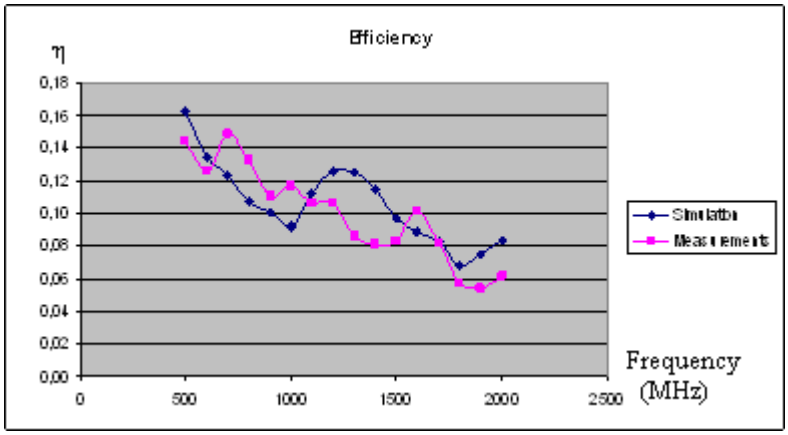

Figure 5.37: Comparison of efficiency results between simulation and measurement for multi stage configuration

From Figure 5.37, it can be seen that, the results of the simulation and the measurement are so close to each other at 33dBm output power.

5.3.5.6. Pout vs. Pin CURVES

The following graphs show the comparison of the P_{out} versus P_{in} curves for the complete system where the input signal frequency is 500MHz, 1000MHz, 1500MHz, and 2000MHz.

at $fc = 500MHz$:

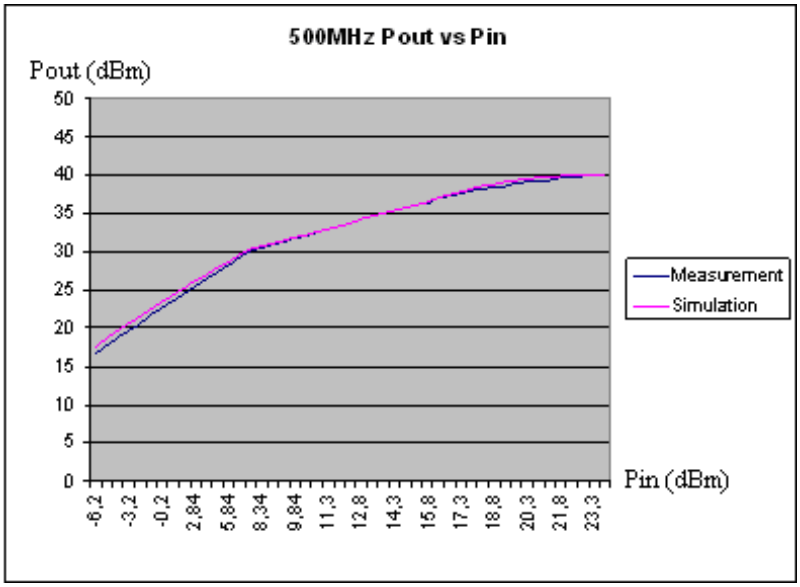

Figure 5.38: Comparison of P_{out} vs. P_{in} results between simulation and measurement at 500MHz for multi stage configuration

at $fc = 1000MHz$:

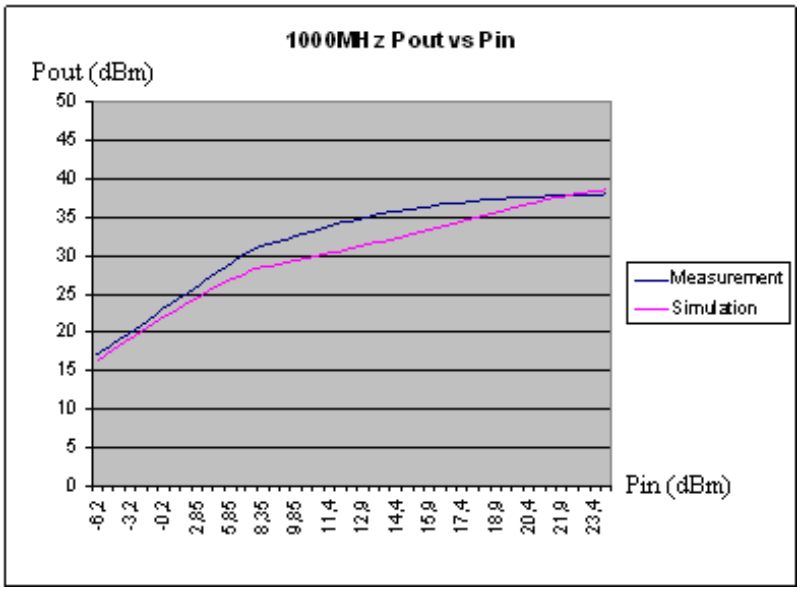

Figure 5.39: Comparison of P_{out} vs. P_{in} results between simulation and measurement at 1000MHz for multi stage configuration

at $fc = 1500MHz$:

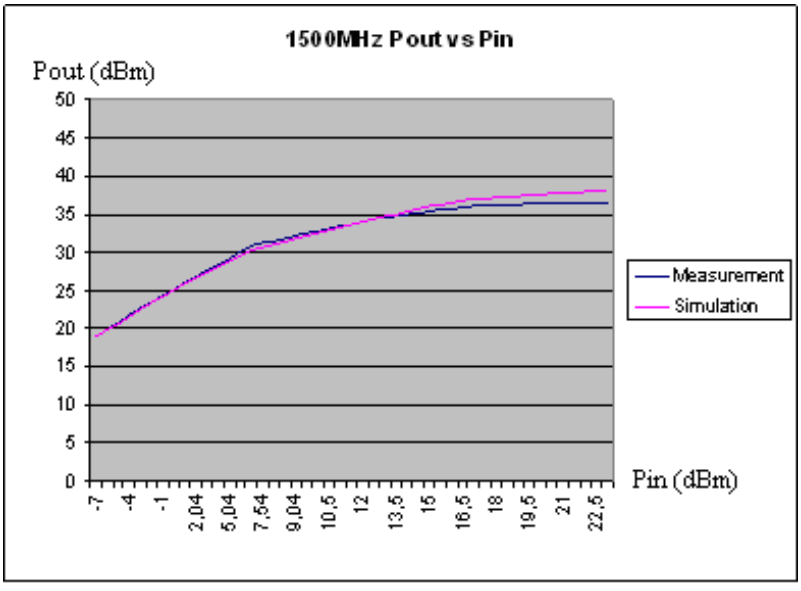

Figure 5.40: Comparison of P_{out} vs. P_{in} results between simulation and measurement at 1500MHz for multi stage configuration

at $fc = 2000MHz$:

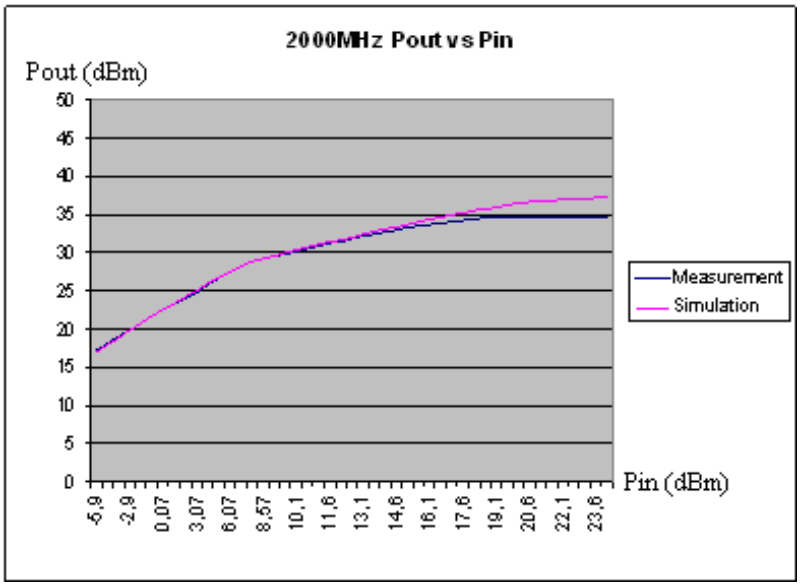

Figure 5.41: Comparison of P_{out} vs. P_{in} results between simulation and measurement at 2000MHz for multi stage configuration

From the above figures it can be seen that the results of simulation and measurement deviate from each other at some frequencies and at some input levels. Although this difference occurs at some conditions, it can be said that the complete system is properly modeled into simulation

5.4. SUMMARY

In this section we analyzed the complete system of the power amplifier. In last stage, LDMOS transistor technology is chosen again, and the reason of choosing this technology was told in the previous sections.

If we look at the results of simulation and measurement in comparison, it can be said that the circuitry in simulation is properly modeled according to the results of measurement. When IMD results of them are analyzed, it can be said that non-linear

characteristics of the system in both simulation and measurement are very similar to each other. Although, P_{out} vs. P_{in} results in both simulation and measurement deviate at some frequencies, in general they seem to be same. In simulation the amplifier produce more output power than in measurement. Because there is no temperature rising in simulation, but in measurement when the transistor begins to heat, its maximum output power reduces. I think that this is the reason of the difference of P_{out} vs. P_{in} results at some frequencies.

Parasitic effects of the system are tried to model in the simulation. In this process, the models of the lumped components are put in simulation and pad parasitic of them are tried to analyze. The ground area at the bottom side of the RF Choke pads and the transistor drain pad are removed to reduce the parasitic effects.

The output matching network of the complete system is tried to optimize in measurement process, because at the beginning of the project we made simulations of the complete circuitry, and we found the length and width values of the microstrip lines and open circuit stubs in simulation, then we design our printed circuit board according to the values taken from simulations. When the whole system is analyzed on PCB, we see that the result of output return loss isn't expected, so we try to optimize the output matching network by modifying the length and width of the microstrip lines and open circuit stubs on PCB. Final simulation modeling process is done according to the length and width values found in measurement.

If we look at the graphs which compare the results of simulations and measurements, in previous section; it can be seen that the power amplifier circuitry is modeled when large signal input level is applied. It means that non-linearity of the system is considered when the circuitry is modeled into simulation.

CHAPTER VI

CONCLUSION

In this thesis, the methods of designing a broadband power amplifier are investigated and also nonlinear modeling techniques are presented. The power amplifier circuitry is tried to model in simulation according to the results of measurements. The results of measurement are taken when large signal condition is applied to the circuitry, and according to these large signal results the circuitry is modeled in simulation.

The power amplifier design process begins with searching RF power transistors and suitable printed circuit board material. The transistor technologies of Si CMOS, Si LDMOS, GaAs MESFET, GaAs PHEMT, GaAs MHEMT, GaAs HBT, InP HEMT, InP HBT, SiC MESFET, SiC LDMOS, SiGe HBT, and GaN HEMT are analyzed thoroughly and the suitable one, Si LDMOS, is chosen according to the criterias which are presented in Chapter III. The amplifier is designed as it has two stages, and in both stages, LDMOS transistor is used as RF power transistors. For driver stage; Freescale Company's MW6S004NT1, and for last stage; NXP Company's BLF3G21-6 LDMOS transistors are used. After choosing the RF transistors, PCB material that is suitable for the amplifier operating frequency band, is searched and Rogers RO4003C is chosen (see Table 4.1).

Initially, the driver stage and then the last stage are designed, so the complete power amplifier system is obtained. A broadband RF-Choke structure with a new technique is developed to obtain high DC isolation and low RF loss over the desired bandwidth. The inductance of the RF-Choke is split up into two series connected elements to overcome the parasitic capacitive coupling problems. Besides, the ground area of the PCB at the bottom side of the RF-Choke pads is removed to reduce the parasitic effects. Thus, a sufficiently high self resonance frequency (SRF) is obtained. Moreover, in order to reduce the parasitic effect of the RF transistors, the ground area of the PCB at the bottom side of the drain pads is removed.

In both design steps (these are designing of driver stage and design of complete system); the simulation and measurement results are taken and non-linear modeling process is done. Large signal models for the LDMOS devices are used in simulation, and according to the measurement results, the circuitry in simulation is tried to be modeled at nonlinear conditions. The models of the lumped components are used in simulation and pad parasitics of them are tried to be analyzed. Pad parasitics of the lumped components are tried to be modeled as a capacitor and a resistor in series is connected in parallel to the lumped component (because one lumped component uses two pads on PCB for soldering). The values of these resistances and capacitances are determined according to the size of the pads used on PCB for the lumped components.

The comparable results of simulation and measurement are presented for both the design of the driver stage and the multistage sections. It is seen that the simulation and measurement results are so close. Typical values of 20dB power gain and 37dBm output power have been achieved in most part of the frequency band of 500MHz-2GHz.

As a result of this thesis, it can be realized that at this frequencies the parasitic effects increase and it becomes a crucial factor for designing a system. Choosing a suitable PCB material is so critical to reduce parasitics, because every PCB material has its own operation frequency band. On the other hand, the ground areas that are close to the RF transmission line, have to be removed to reduce RF coupling. It can be also realized that Silicon LDMOS transistor is not suitable for being used as an RF power transistor for 500MHz-2GHz power amplifier application; however, it can work up to 1.5GHz. Its input and output impedances are seen too scattered in Smith Chart in 1.5GHz-2GHz frequency band, that it can be very hard to match input and output termination of the transistor to 50Ω in 1.5GHz-2GHz frequency band. Insufficiency of matching in this frequency band causes the transistor efficiency getting worse, and also reduces the maximum output power that the transistor is able to provide in 1.5GHz – 2GHz frequency band.

In the future, a 500MHz-2GHz power amplifier can be designed by using other transistor technologies (i.e. GaN, SiC or GaAs). By using any other suitable transistor technology, better matching can be achieved so the results can be better. Furthermore, in order to obtain higher output power, this amplifier can be designed by using In Phase or Quadrature Coupled Power combiners.

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APPENDIX

HARMONIC BALANCE METHOD

The Harmonic Balance technique is an iterative technique which seeks to match the frequency components (harmonics) of current in a set of branches joining two subcircuits. Duality principle can be applied to this technique. It can match the voltage on either side of the nodes. The branches are chosen in a way that nonlinear elements (the nonlinear elements of the quasistatic semiconductor model) are partitioned into one subcircuit and linear elements (input and output matching circuits, linear elements of the model, source and load impedances) into the other, as shown on the Figure 7.1. The N branches at the linear-nonlinear interface connect the two circuits and define corresponding nodes, current flowing out of one circuit must equal that flowing into the other expressed by equation 7.1.

$$\begin{bmatrix} I_1(kw) \\ I_2(kw) \\ . \\ . \\ I_N(kw) \end{bmatrix} = \begin{bmatrix} \overline{I}_1(kw) \\ \overline{I}_2(kw) \\ . \\ . \\ \overline{I}_N(kw) \end{bmatrix} \tag{7.1}$$

Matching the frequency components in each branch satisfies continuity equation for current. The current at each branch is obtained by a process of iteration so that dependencies are satisfied for both the linear and nonlinear side of the circuit.

The nonlinear circuit is generally represented by a nonlinear set of equations.

$$I_j(t) = g(V_1(t),.....V_N(t)) \tag{7.2}$$

Where g is an arbitrary nonlinear function (and can include differentiation and integration) and I_j and V_j are the *jth* branch current and voltage. The dependent variables I_j are nonlinear functions of the independent variables V_j at some point in time T_s. Periodic steady-state operation is assumed so that integrals and derivatives at T_s may be determined.

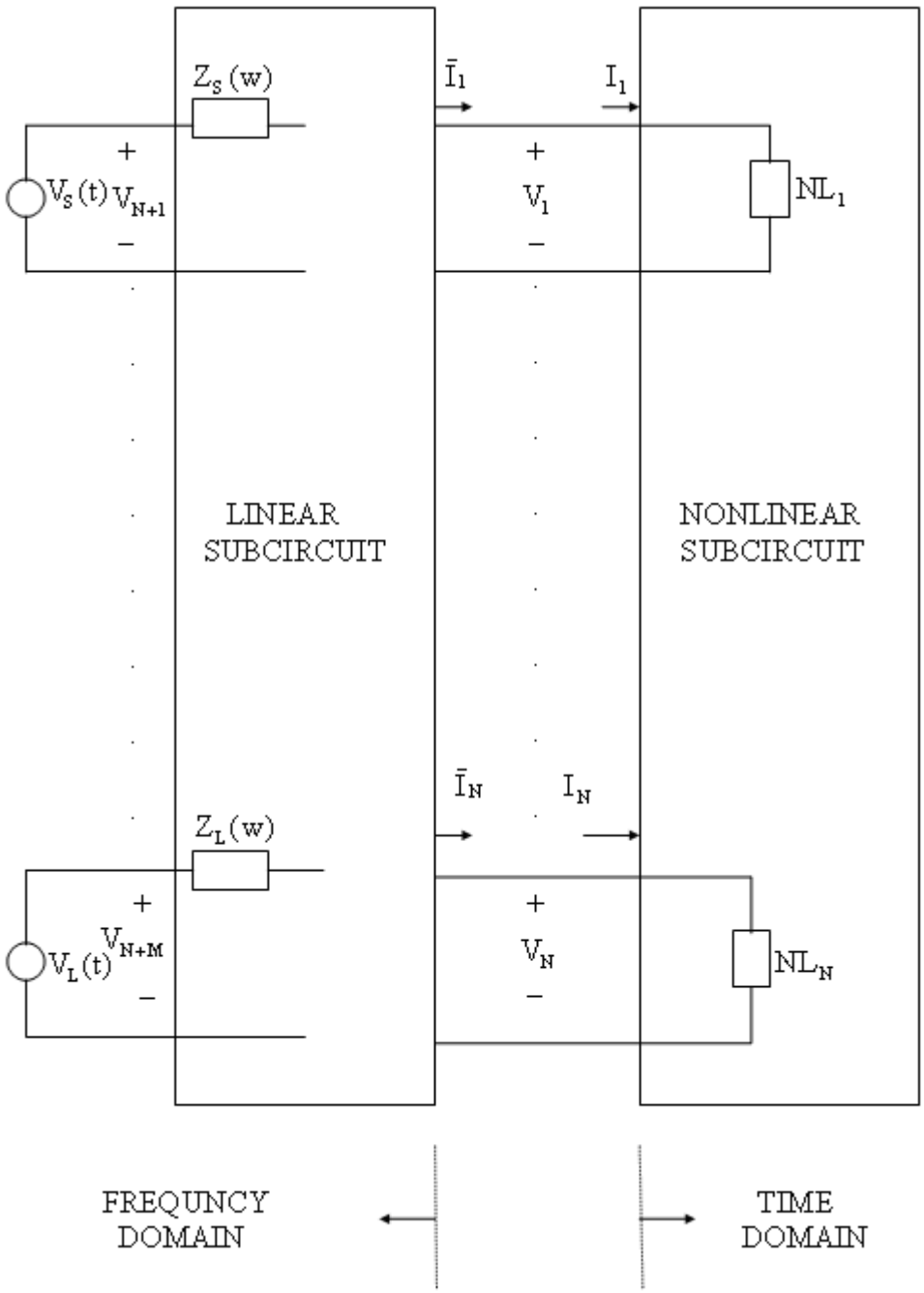

Figure 7.1: Partitioning of circuit into linear and nonlinear subcircuit.

The linear circuit may be represented by an N by N+M matrix obtained by a standard linear circuit analysis method.

The M additional variables are the additional external nodes (or branches) at which applied voltages (or currents) are present. The linear circuit matrix is calculated at each frequency component present in the circuit. In the case of an applied input signal which contains harmonically related components at $w, 2w, ..., wq$ there will be (q+1) matrices relating the independent variables at each branch to the dependent variables.

$$\begin{bmatrix} \mathrm{V}_1(\mathrm{kw}) \\ . \\ . \\ . \\ \mathrm{V}_\mathrm{N}(\mathrm{kw}) \end{bmatrix} = \begin{bmatrix} \mathrm{H}_{11}(kw) H_{12}(kw) ..... H_{1(N+M)}(kw) \\ \mathrm{H}_{21}(kw) H_{22}(kw) ..... H_{2(N+M)}(kw) \\ . \quad . \quad . \\ . \quad . \quad . \\ . \quad . \quad . \\ \mathrm{H}_{\mathrm{N1}}(kw) H_{N2}(kw) ..... H_{N(N+M)}(kw) \end{bmatrix} \begin{bmatrix} I_1(kw) \\ . \\ . \\ I_N(kw) \\ V_{N+1}(kw) \\ . \\ . \\ V_{N+M}(kw) \end{bmatrix} \tag{7.3}$$

for k=0, 1... q

Where the $H_{ij}(kw)$ are impedance or transfer ratios depending on which of the variables are voltages and which are currents. The purpose of the Harmonic Balance method is to find a simultaneous solution to equation (7.2) and (7.3) for $\mathrm{V}_1, \mathrm{V}_2 ..... \mathrm{V}_\mathrm{N}$ so that $I_1, I_2 ..... I_N$ may be determined.

Figure 7.2 illustrates the application of the method to a three terminal device such as a MESFET. Two branches constitute the MESFET gate input and the MESFET drain output. These separate the nonlinear MESFET elements into one subcircuit and the parasitics, matching and output networks into another linear subcircuit. The third branch is the source of the MESFET and is chosen as the reference so that N=2. Here V_1 and V_2 are the independent variables and I_1 and I_2 are the dependent

variables. Additional applied inputs are the external voltages V_1 and V_2. The desired output variables such as current and voltage in the load can be found once I_1 and I_2 are found.

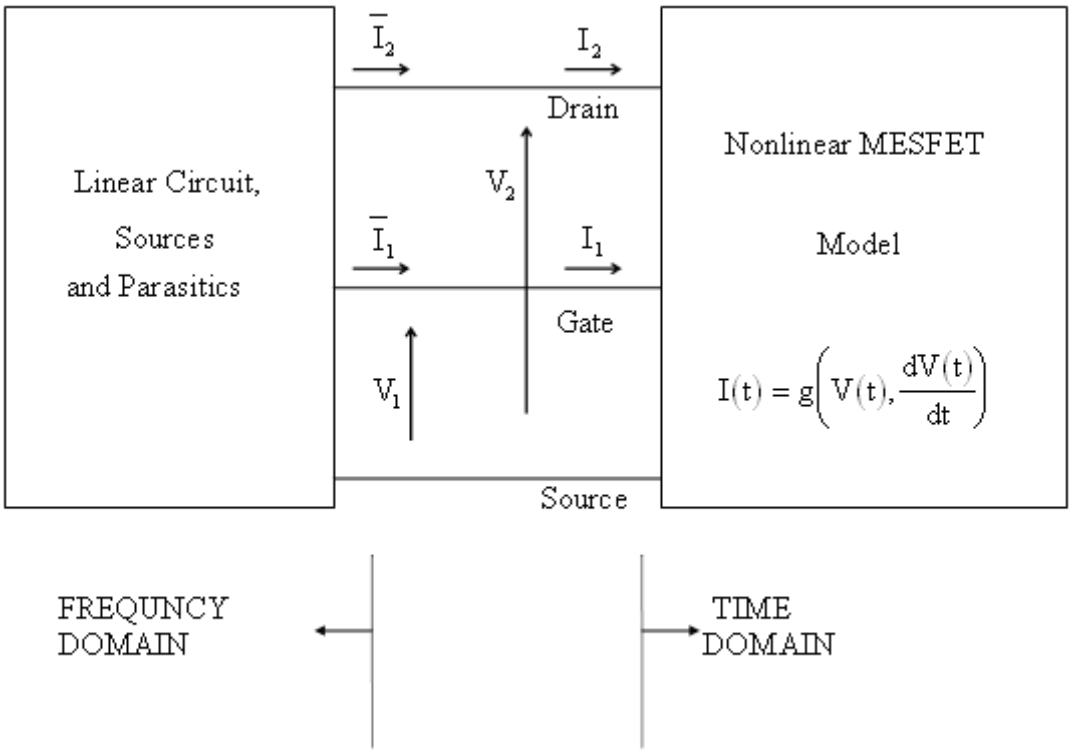

Figure 7.2: Partitioning of a MESFET circuit to subcircuits.

Equation (7.2) is stated in the time domain and (7.3) is stated in the frequency domain. Time-to-frequency conversion is achieved using the Discrete Fourier Transform (DFT). If estimates of $V_j(t)$ for j=1, 2.....N at some T_s are substituted into equation (7.2) I_j can be found at time T_s. If this is done at time instants $T_s, 2T_s, ...LT_s$ an L-point sequence of time samples of I_j results. The Nyquist sampling theorem states that if a sequence of points is obtained by a sampling a waveform at a rate that is at least twice the highest component contained, the

original waveform can be reconstructed. If the wave form contains only discrete frequencies which are spaced by integral multiples of w up to qw one can set

$$T_s = \frac{2}{(2q+1)w} \tag{7.4}$$

with $L = 2q+1$ to satisfy the Nyquist criterion and can extract the desired frequency components at w from the L-point sequence by using the DFT.

An initial estimate must be made for I_j and V_j because they are not known. Iteration between equation (7.2) and (7.3) is performed using the DFT to obtain the frequency components from the time samples obtained from equation (7.2) until a self-consistent set of variables which satisfy the current continuity equations is obtained. The algorithm used in the analysis is as follows (7.5), (7.6).

1. Initial guesses are established for the current phasors $\overline{I}_j(kw)$ at the interface branches at the dc, fundamental, and harmonic frequencies (k=0, 1...q). The overbar refers to the current flowing in the linear side of the interface branches.

2. The hybrid matrix for the linear circuit $H(kw)$ is calculated at dc, the driving frequency w, and each harmonic. This is used with $\bar{I}_j(kw)$ and the applied external voltages in equation (7.3) to calculate the unknown phasor components of voltage at each of the N branches.

3. Using an expression

$$V_j(t) = \text{Real}\sum_{k=0}^{q} V_j(kw)e^{jkwt} \tag{7.5}$$

to derive the time value of the branch voltages at times t= $T_s, 2T_s, ...LT_s$ and a similar expression for derivatives, the time samples of voltage and its derivatives may be calculated at each of N branches.

4. Values of $I_j(t)$ in the nonlinear side of the interface branches may be obtained at corresponding time instants by substitution of the time samples of voltage $V_j(t)$ and its derivatives into equation (7.2).

5. Using the DFT, the harmonic phasor components $\bar{I}_j(kw)$ may be extracted from the L-point sequence of $I_j(t)$ because the sequence consists of samples obtained at the Nyquist rate.

6. An error function is formed to compare the nonlinear current estimates I_j with the linear estimates $\bar{I}_j$.

$$E = (I_1, ..I_N, \bar{I}_1, ..\bar{I}_N) = \sum_{k=0}^{q} (|I_1(kw) - \bar{I}_1(kw)|^2 + .. + |I_N(kw) - \bar{I}_N(kw)|^2) \quad (7.6)$$

7. The continuity equation for current states that the nonlinear currents must equal the linear currents. This corresponds to zero error function as a solution. The error function is minimized by forming new initial guesses for the current phasors $\bar{I}_j(kw)$ from the old estimates and repeating steps 2. through 7. until the error function is below some threshold. At this point, the linear and nonlinear partitions give self-consistent results, since the currents on each side of the interface branches are equal.

There are many algorithms for solving the Harmonic Balance iterations such as Reflection algorithm, Newton's method, Relaxation method. The fixed-point method of Hicks and Khan (7.7), (7.8) which is called as Relaxation or Splitting method is used here to achieve convergence and force the function to zero (error function) by allowing the phasor currents to more closely approximate their true values on successive iterations. After the r_{th} iteration of the loop, consider the current in the j_{th} branch.

$$I_{jr}(t) = \sum_{k} I_{jr}(kw) e^{jkwt} \tag{7.7}$$

with corresponding

$$\bar{I}_{jr}(t) = \sum_{k} \bar{I}_{jr}(kw) e^{jkwt} \tag{7.8}$$

The next iteration is then carried out with $\bar{\mathrm{I}}_{\mathrm{j(r+1)}}(\mathrm{kw})$ formed by

$$\bar{I}_{j(r+1)}(kw) = \mathrm{p}\ I_{jr}(kw) + (1\text{-p})\ \bar{\mathrm{I}}_{\mathrm{jr}}(\mathrm{kw}) \tag{7.9}$$

Where p is determined by convergence considerations and $0<P\leq 1$.

The value of the parameter p has a strong effect on the convergence properties of the process. Small values of p result in relatively slow but reliable convergence, large values result in much greater modification of $\mathrm{I_j}$ per iteration, but increase the chance that the process will diverge.

CONVERGENCE CONSIDERATIONS

There are critical properties of the iterative analysis which are its speed, the reliability of its convergence and the accuracy of the solution. Each algorithm has its own properties. So, the suitable method of iteration depends on the application.

The number of harmonics N is a trade-off between speed and accuracy. A large N improves the accuracy at the expense of slower analysis, while a small N improves speed of the analysis at the expense of accuracy. In general, the optimum N depends on the level of excitation and the type of nonlinearity (weakly or strongly). For the strongly nonlinear circuits, the number of harmonics used in the analysis must be chosen large. However for large N the time required to perform DFT is large.

The trade-off between solution methods is between speed per iteration and degree of convergence per iteration. Methods that are relatively fast per iteration usually require more iterations, while those that are slow improve the error function much more on each iteration.

The Relaxation method is relatively fast per iteration, but convergence is linear at best condition, so it requires many iterations to reach a solution.

Newton's method is quadratically convergent. The number of significant digits in the components of the solution vector approximately doubles at each step. But, each step requires the inversion of a large matrix and is slow. The advantage of the Newton's method is that, with a good initial estimate, its convergence is fairly complete and accurate (7.9).

ACCURACY OF THE HARMONIC BALANCE ANALYSIS

The accuracy of the method is dominated by the number of frequency components used, the properties of the Fourier transforms and the accuracy of the nonlinear device model used. The accuracy increases as the number of harmonics increases (7.9), (7.2) [27].